UNIVERSIDADE ESTADUAL DO OESTE DO PARANÁ - UNIOESTE

CENTRO DE ENGENHARIAS E CIÊNCIAS EXATAS - CECE

CIÊNCIA DA COMPUTAÇÃO

DISCIPLINA: SISTEMAS DIGITAIS

DOCENTES: JORGE HABIB E ANTONIO HACHISUCA

ISABELA PIMENTEL LOEBEL

LISTA DE EXERCÍCIOS 2 -

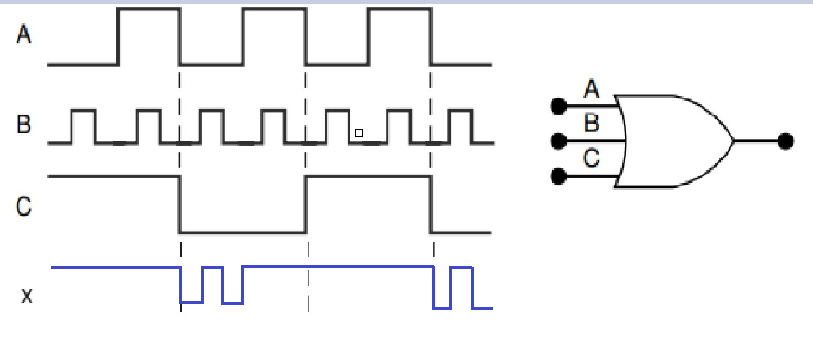
DESCREVENDO CIRCUITOS LÓGICOS

FOZ DO IGUAÇU,

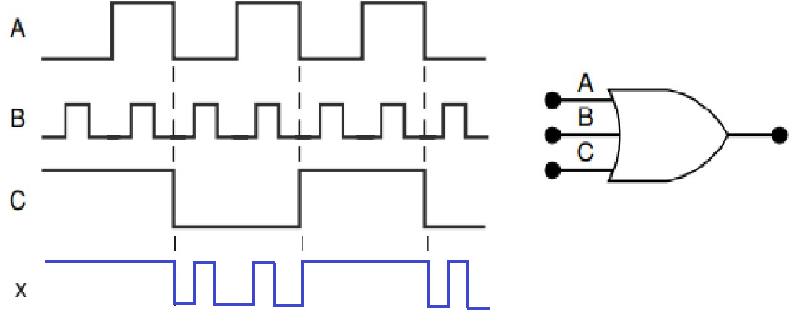
2020.

**Parte I - Livro Ronald J. Tocci**

B 3.1\* Desenhe a forma de onda de saída para a porta OR da Figura 3.52.

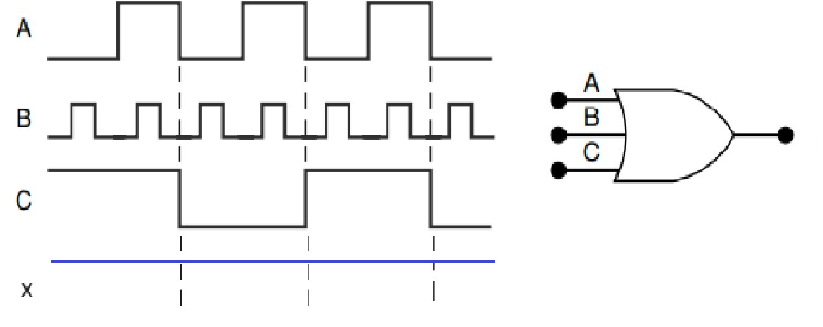


B 3.2 Suponha que a entrada A na Figura 3.52 seja, não intencionalmente, curto-circuitada para o terra (isto é, A = 0). Desenhe a forma de onda de saída resultante.



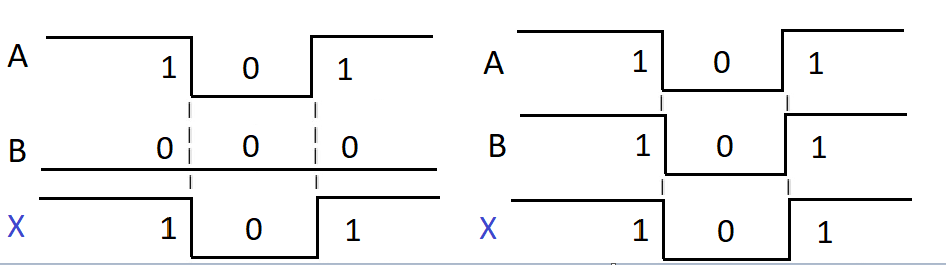
B 3.3\* Suponha que a entrada A na Figura 3.52 seja, não intencionalmente, curto-circuitada para a linha de alimentação +5 V (isto é, A = 1). Desenhe a forma

de onda de saída resultante.

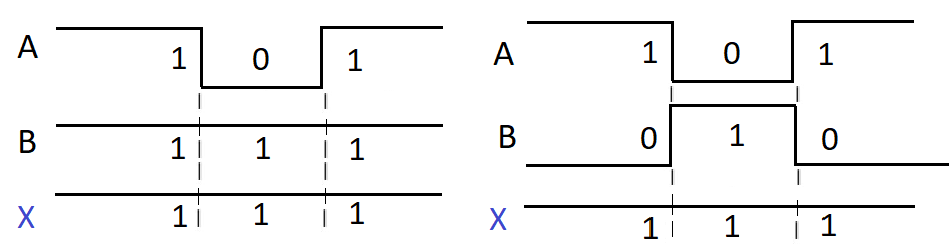


C 3.4 Leia as afirmações a seguir referentes à porta OR. À primeira vista, parecem ser verdadeiras, mas depois de uma análise, você verá que nenhuma é *totalmente* verdadeira. Prove isso com um exemplo específico que refute cada afirmativa.

(a) Se a forma de onda de saída de uma porta OR for a mesma que a de uma das entradas, a outra entrada está sendo mantida permanentemente em nível BAIXO.



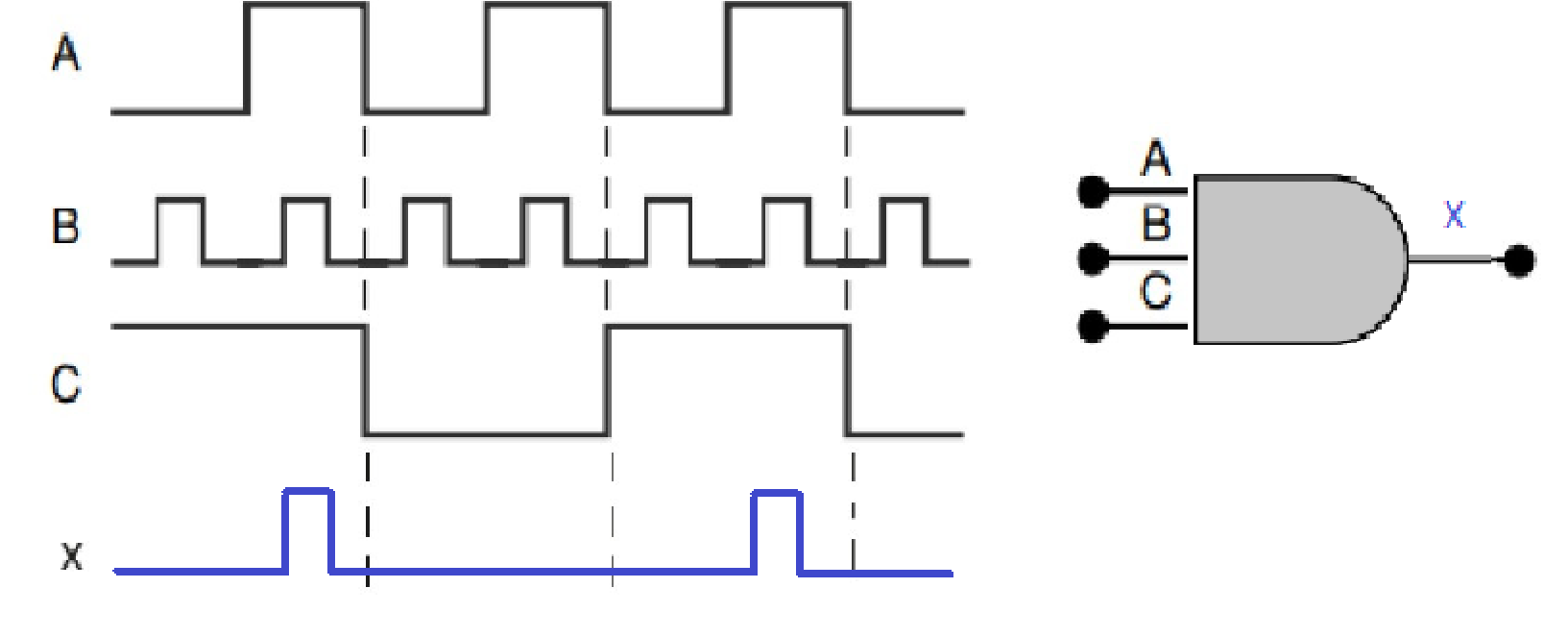
(b) Se a forma de onda de saída de uma porta OR for sempre nível ALTO, uma de suas entradas está sendo mantida sempre em nível ALTO.



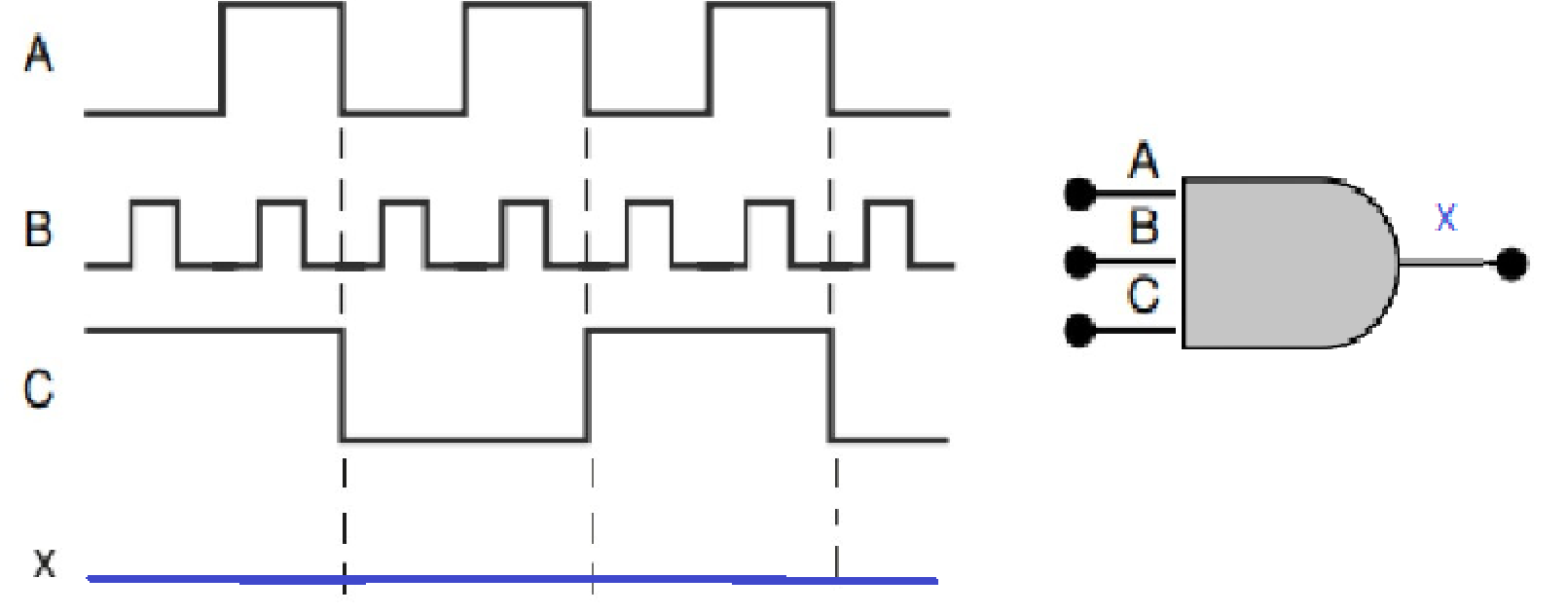
B 3.5 Quantos conjuntos diferentes de condições de entrada produzem uma saída em nível ALTO em uma porta OR de cinco entradas?

R: conjuntos.

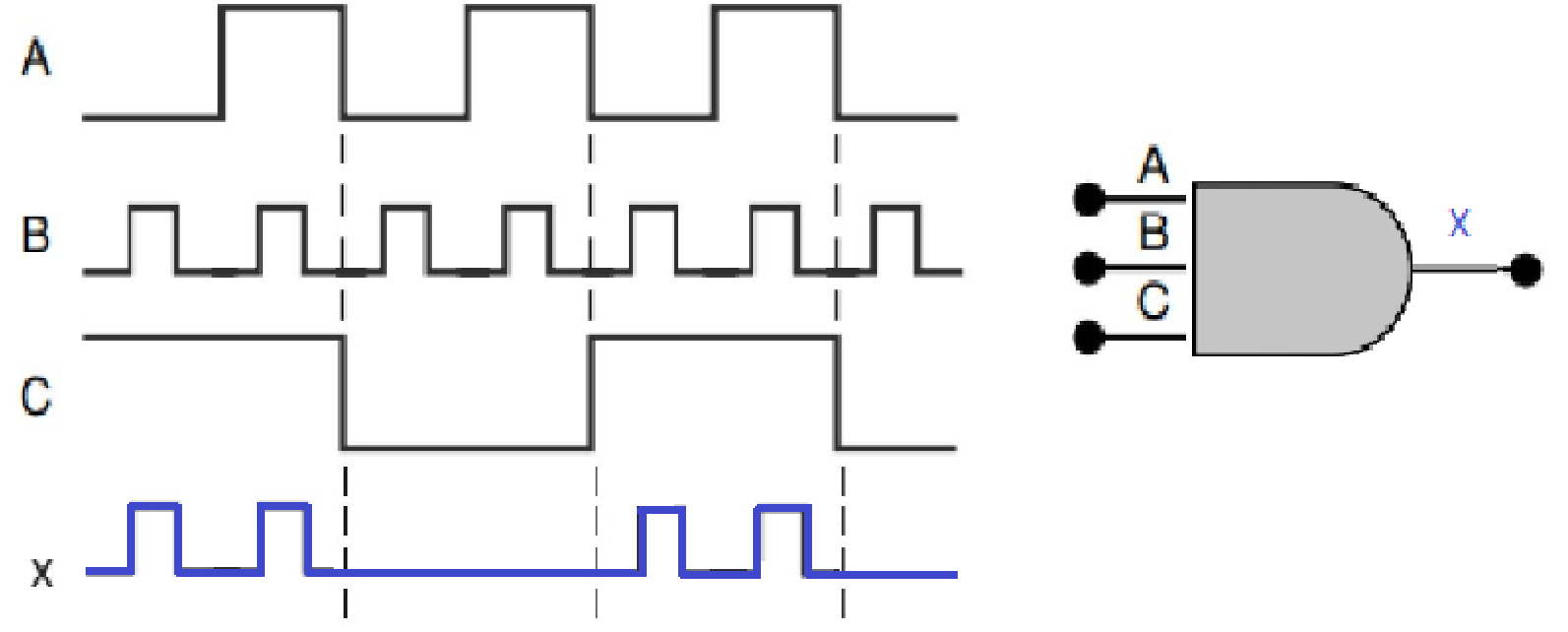
B 3.6 Troque a porta OR na Figura 3.52 por uma porta AND.

(a)\* Desenhe a forma de onda de saída.

(b) Desenhe a forma de onda de saída se a entrada A for permanentemente curto-circuitada para o terra.



(c) Desenhe a forma de onda de saída se a entrada A for permanentemente curto-circuitada para +5 V.



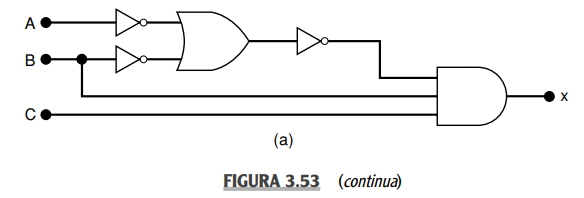
B 3.9 Suponha que você tenha uma porta de duas entradas de função desconhecida que pode ser uma porta OR ou uma porta AND. Qual combinação de níveis de entrada você colocaria nas entradas da porta para determinar seu tipo?

R: Poderia ser colocado a combinação ALTA e BAIXA ou vice-versa, já que se fosse uma porta OR o resultado seria um nível ALTO e se fosse uma porta AND o resultado seria um nível BAIXO.

B 3.10 *Verdadeiro ou falso:* uma porta AND, não importa quantas entradas tenha, produzirá uma saída em nível ALTO para apenas uma combinação de níveis de entrada.

R: Verdadeira, sendo essas entradas todas altas, caso contrário, todos os resultados seriam de níveis baixos.

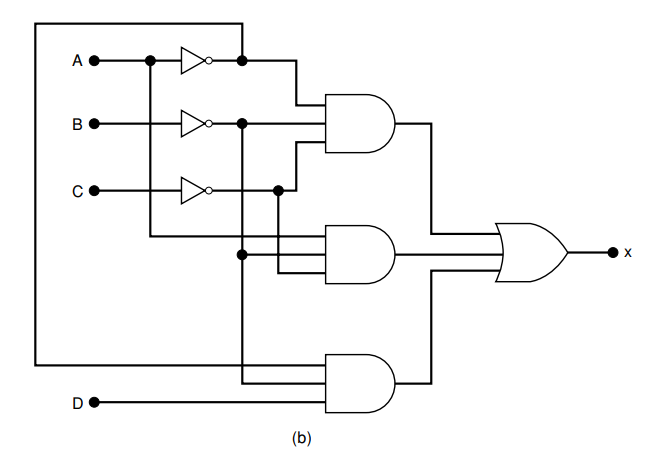
B 3.12 (a)\* Escreva a expressão booleana para a saída x na Figura 3.53(a). Determine o valor de x para todas as condições possíveis de entrada e relacione os resultados em uma tabela-verdade.



R:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

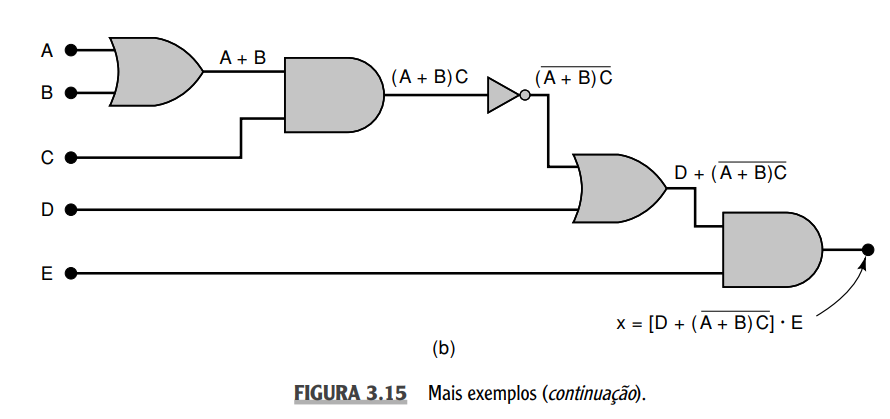
(b) Repita para o circuito da Figura 3.53(b).



R:

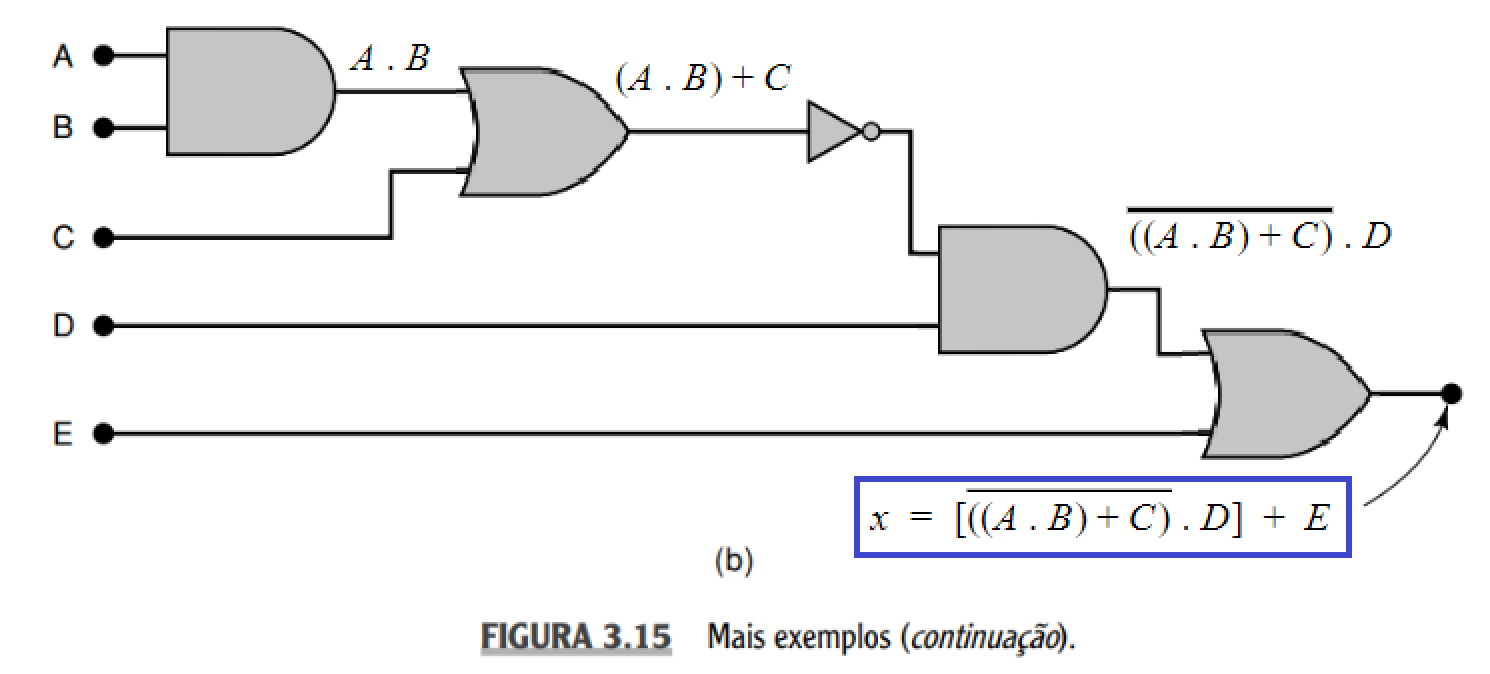
|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

B 3.13\* Determine a tabela-verdade completa para o circuito da Figura 3.15(b) encontrando os níveis lógicos presentes na saída de cada porta para as 32 combinações possíveis de entrada.



|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

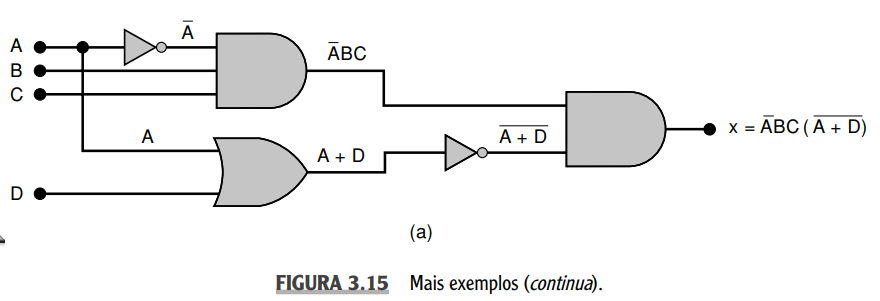
B 3.14 (a)\* Troque cada OR por AND e cada AND por OR na Figura 3.15(b). Em seguida, escreva a expressão para a saída.



(b) Determine a tabela-verdade completa.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
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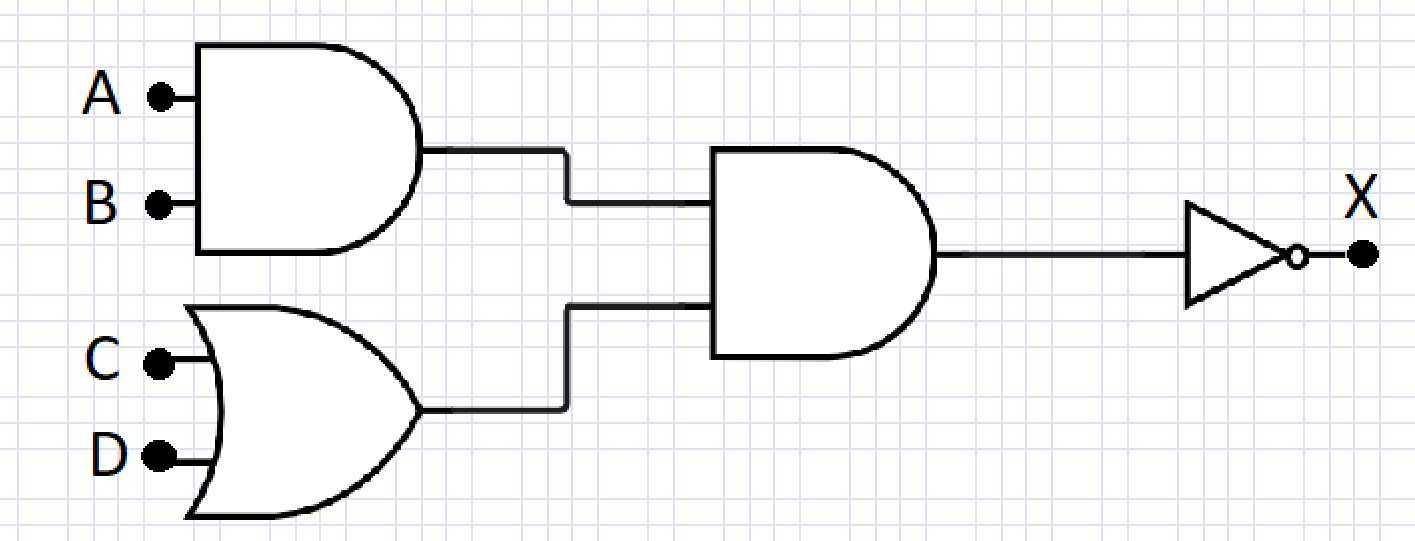
B 3.15 Determine a tabela-verdade completa para o circuito da Figura 3.15(a) encontrando os níveis lógicos presentes na saída de cada porta para as 16 combinações possíveis de entrada.



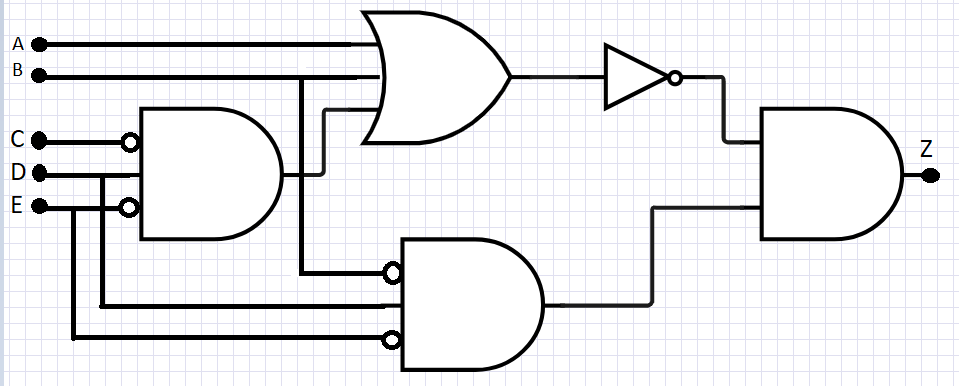
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

B 3.16 Para cada uma das expressões a seguir, desenhe o circuito lógico correspondente usando portas AND, OR e INVERSORES.

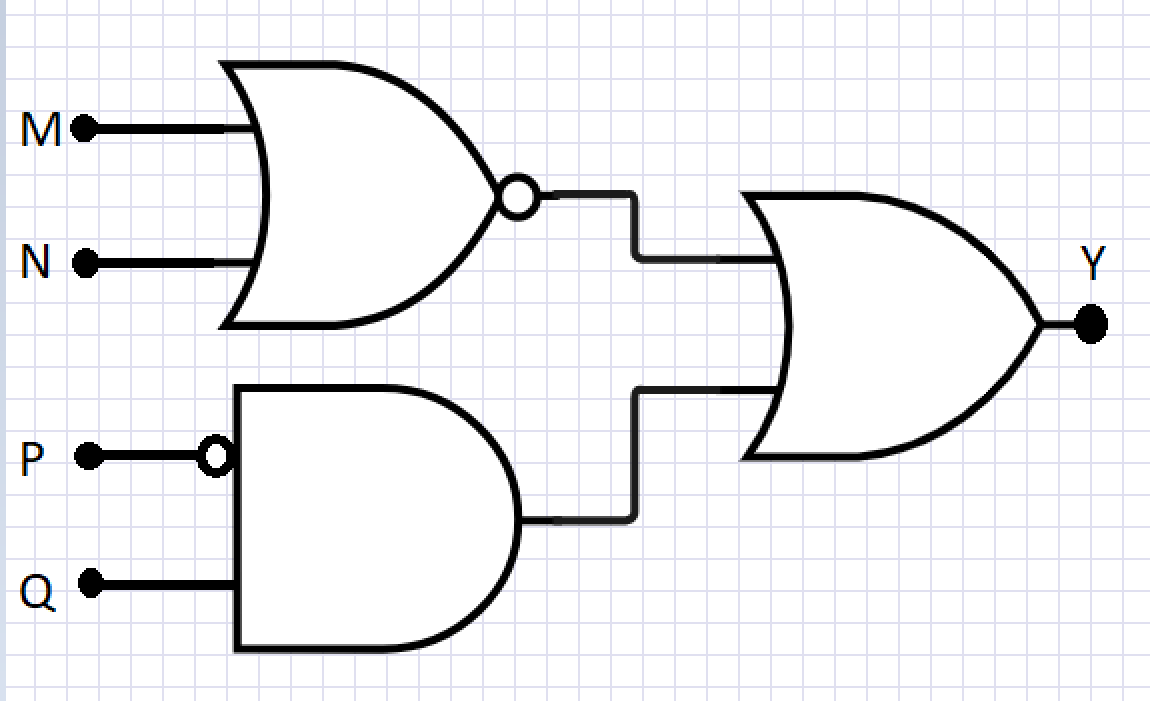
(a)\*



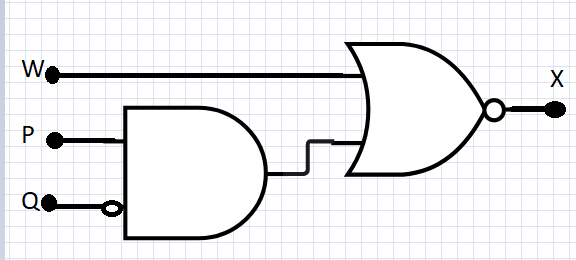
(b)\*



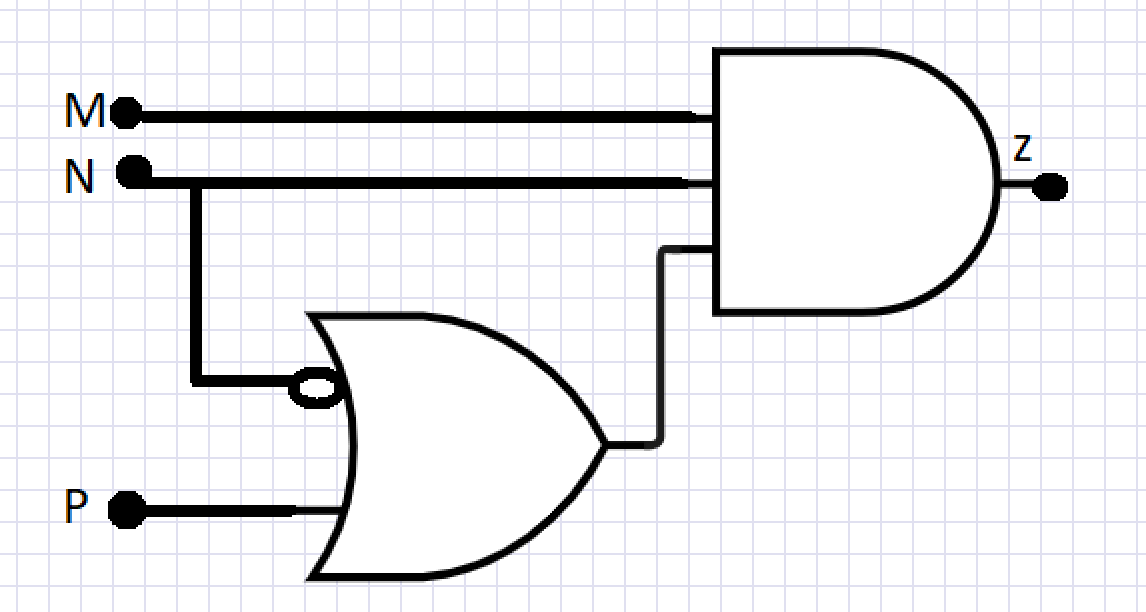
(c)



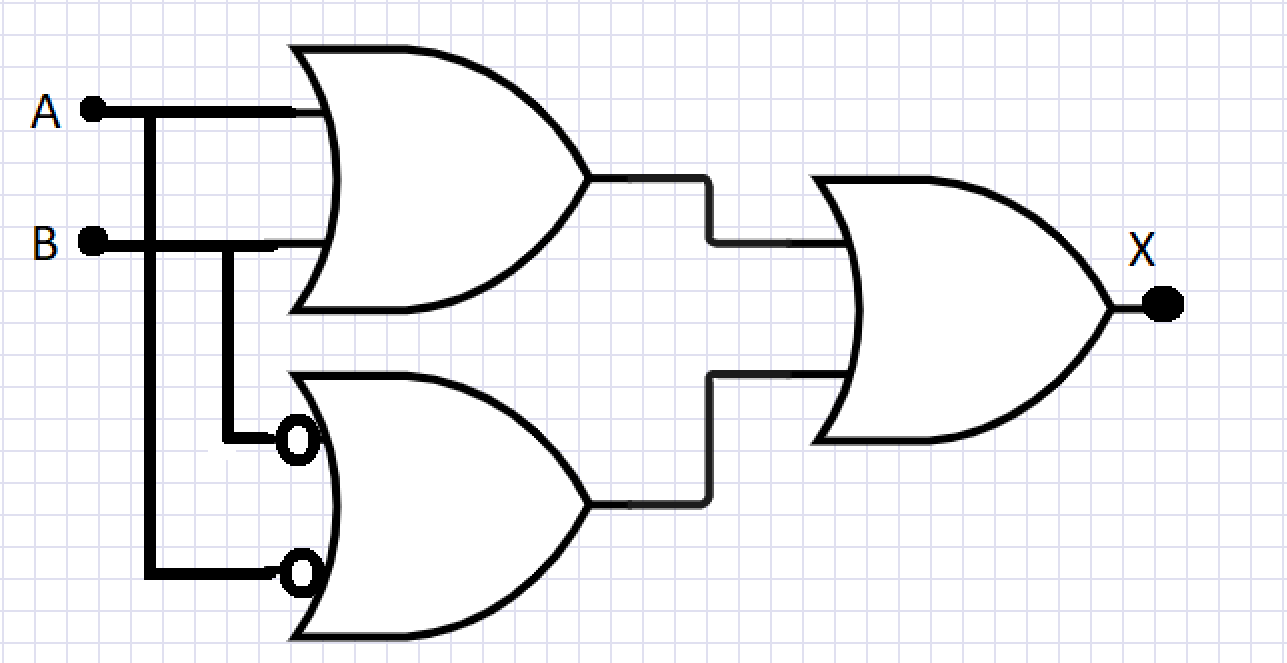
(d)



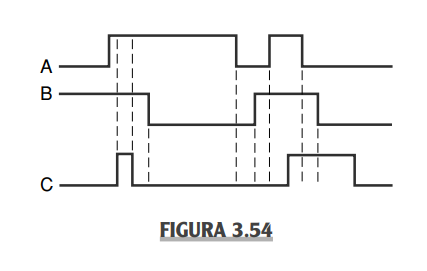
(e)

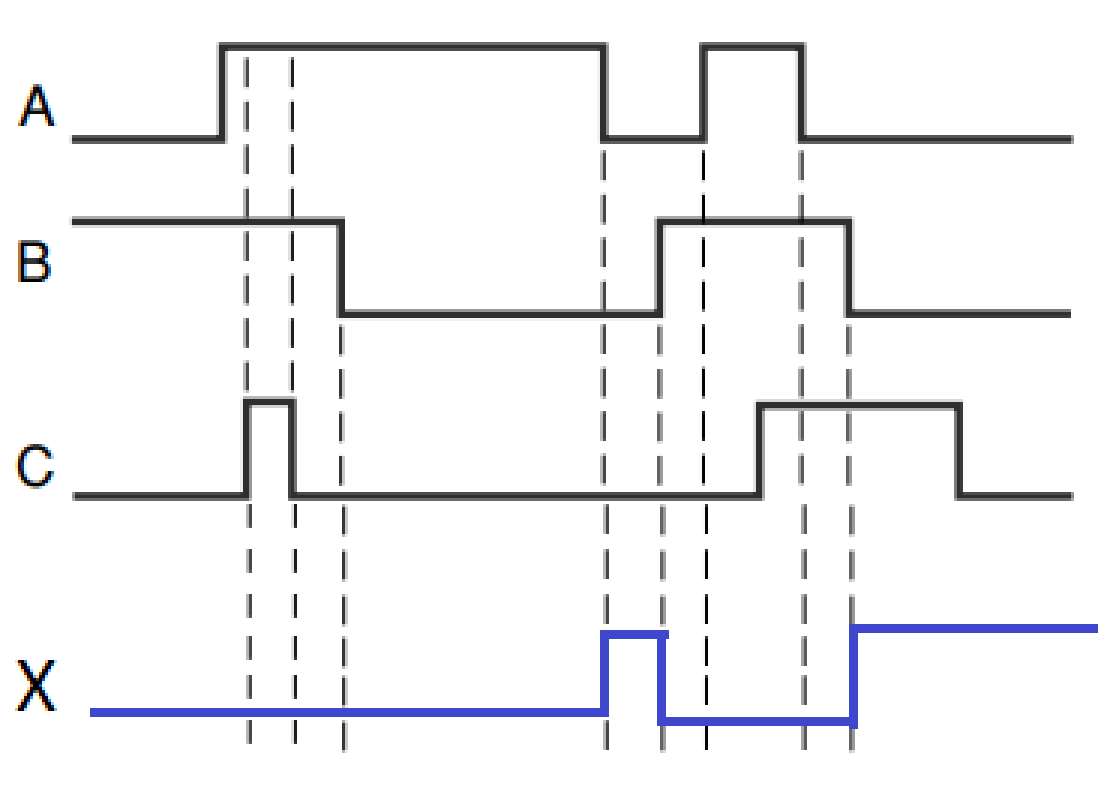


(f)

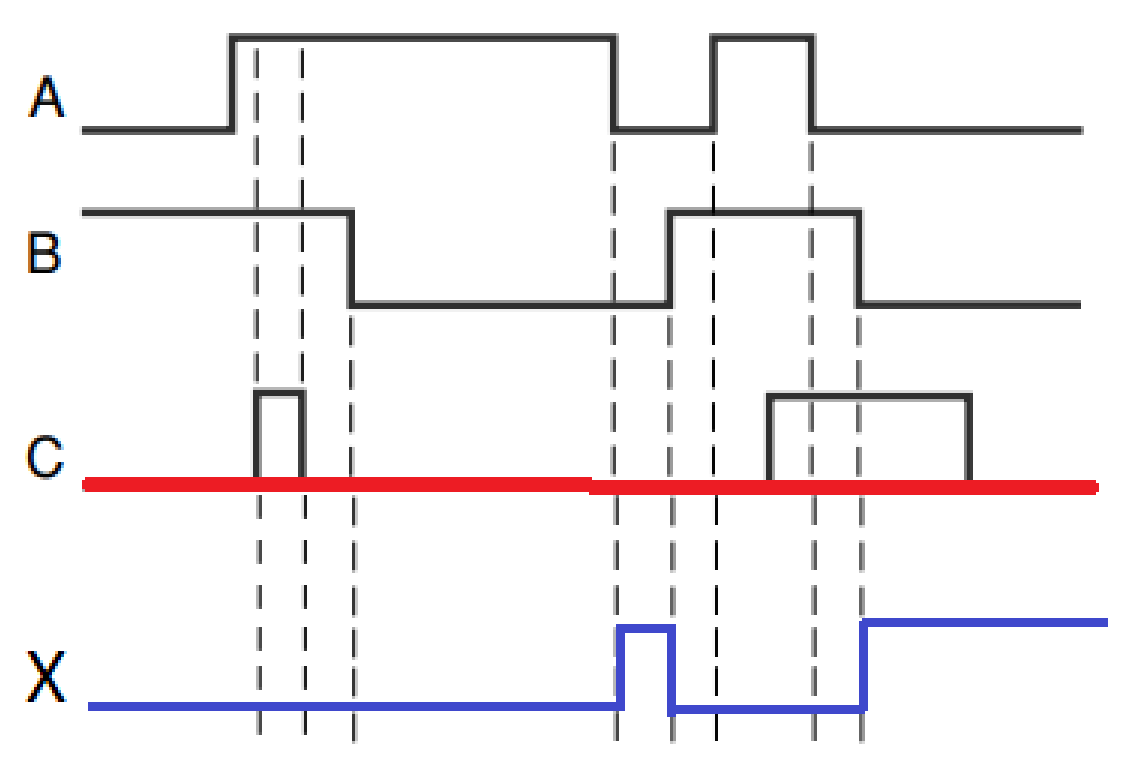


B 3.17\* (a) Aplique as formas de onda de entrada da Figura 3.54 em uma porta NOR e desenhe a forma de onda de saída.

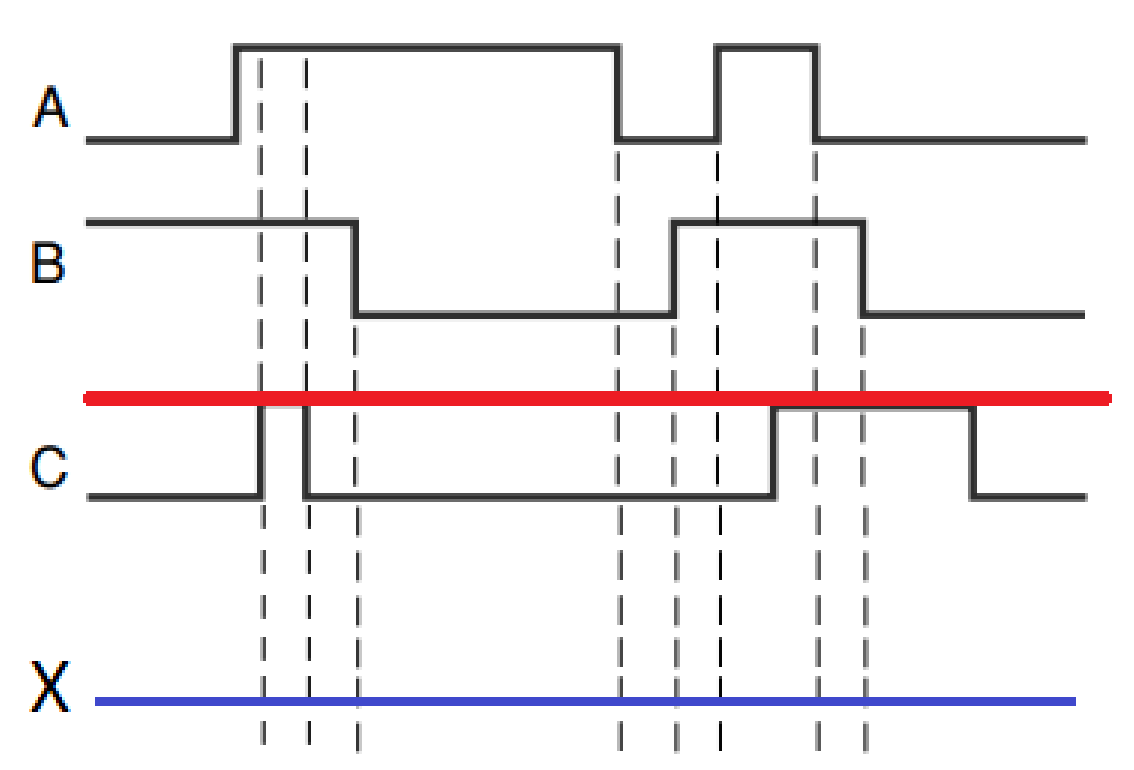




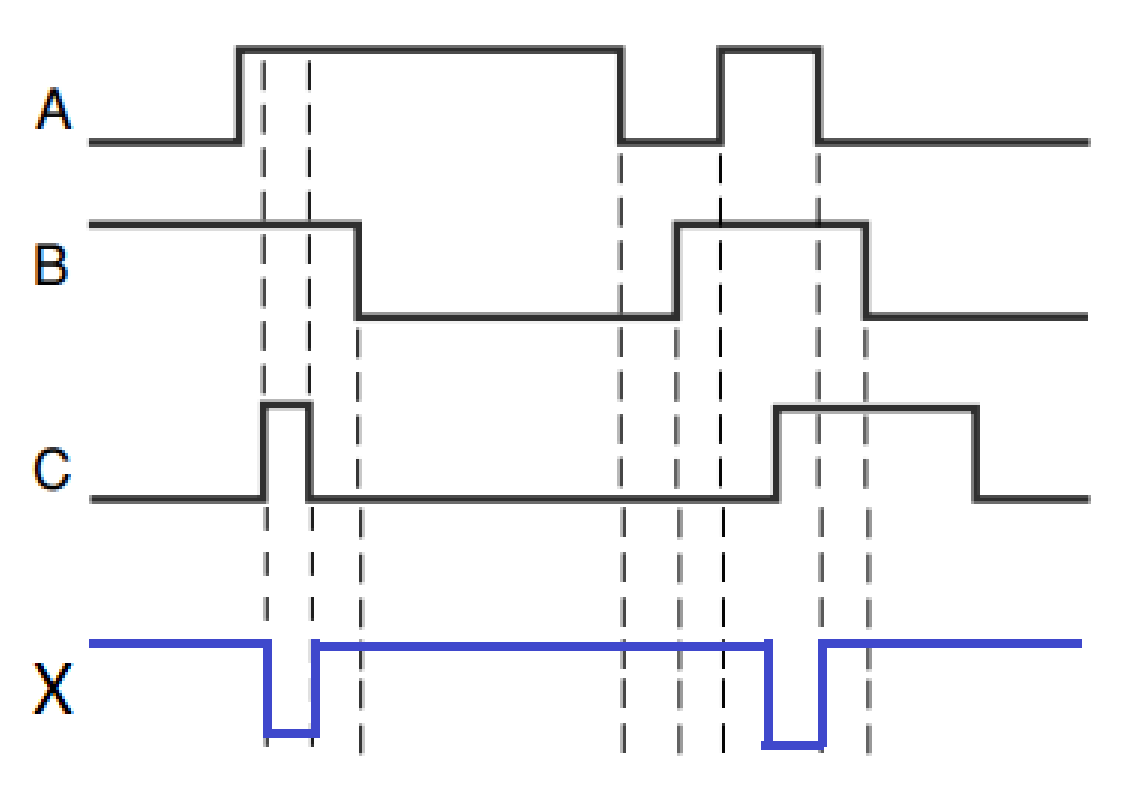
(b) Repita para a entrada C mantida permanentemente em nível BAIXO.

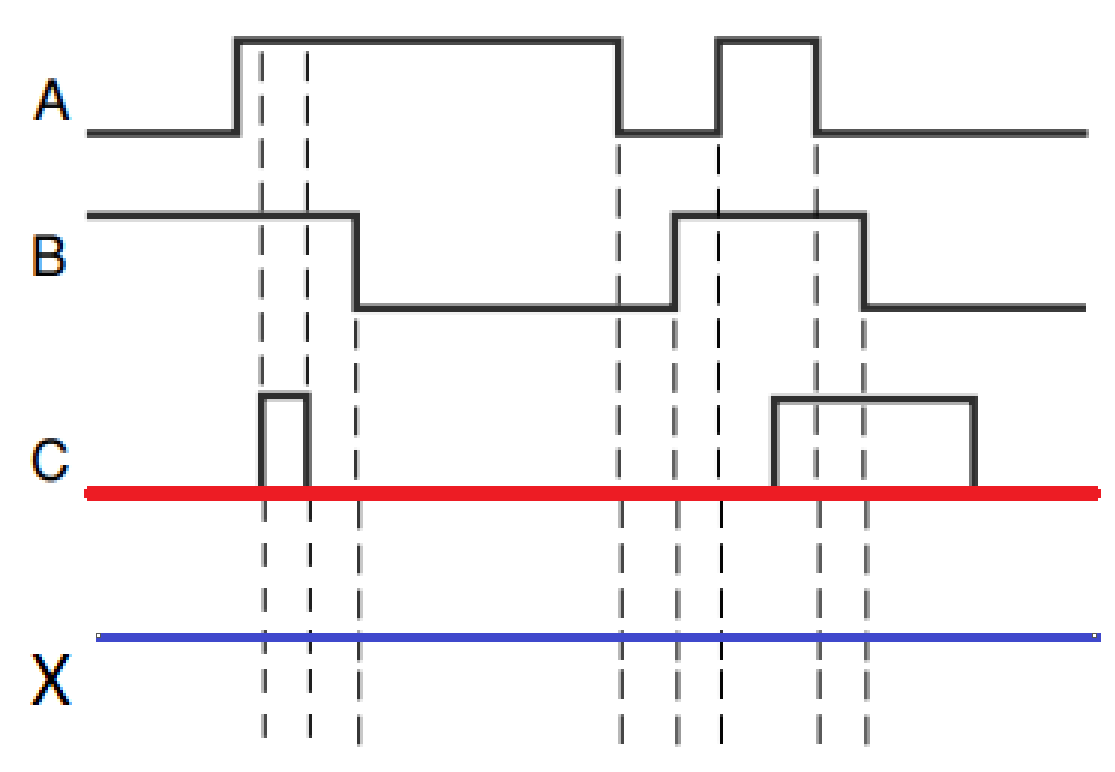


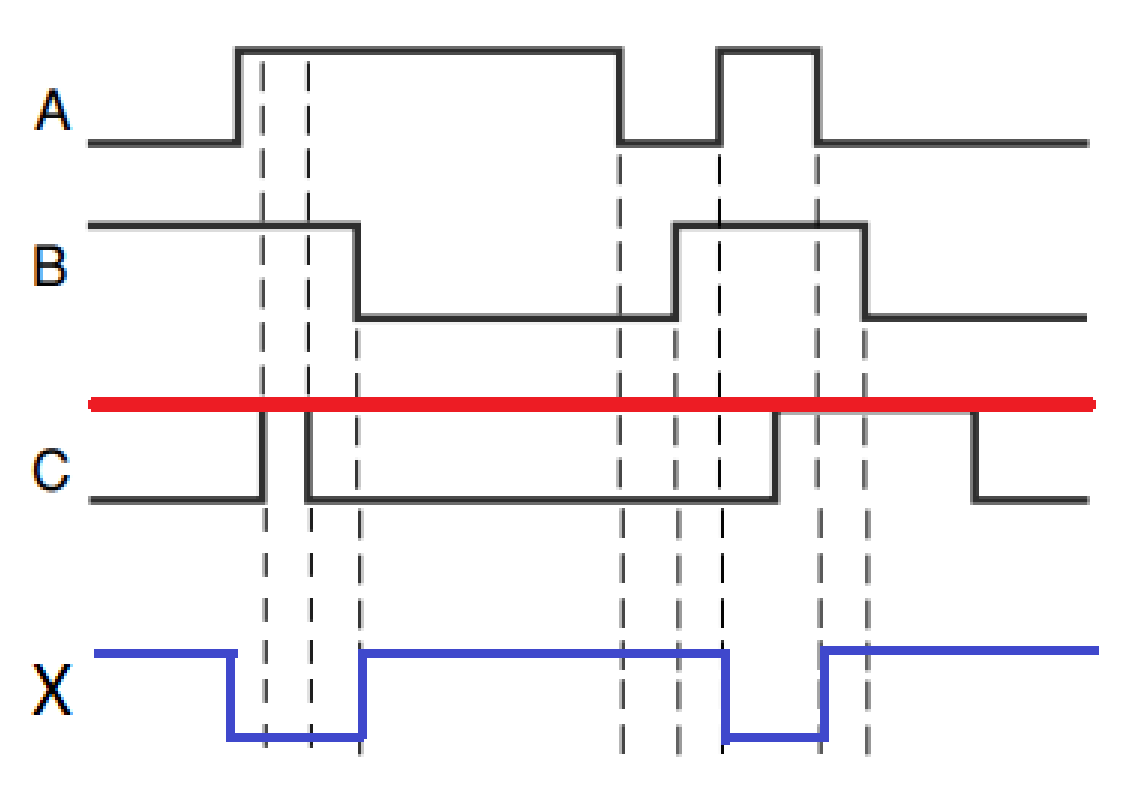
(c) Repita para a entrada C mantida em nível ALTO.



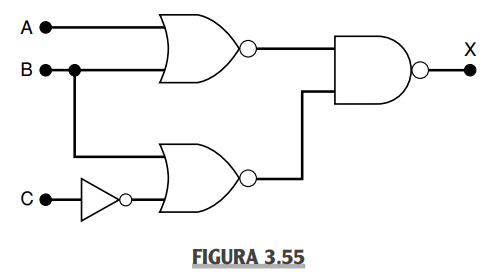
B 3.18 Repita o Problema 3.17 para uma porta NAND.





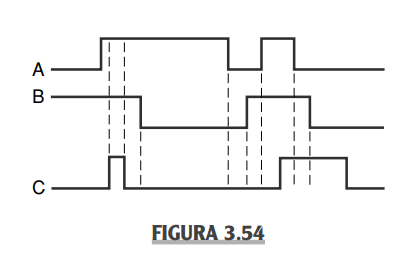
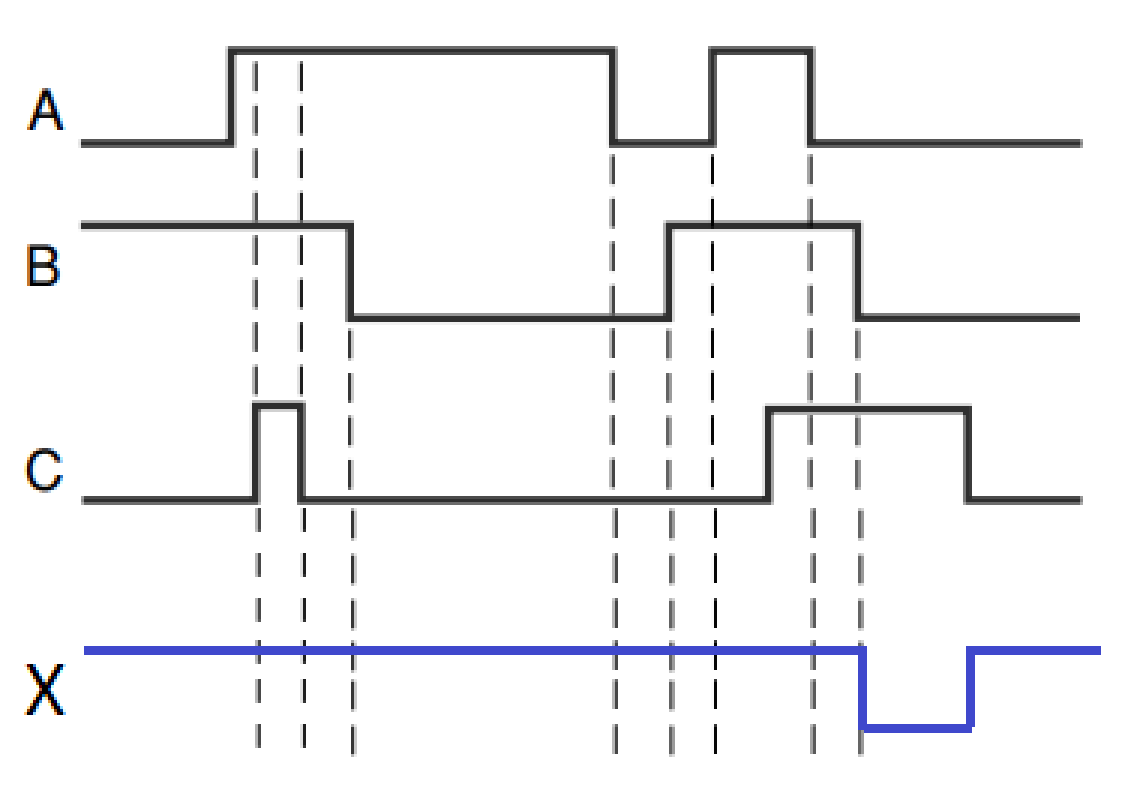


C 3.19\* Escreva a expressão para a saída do circuito da Figura 3.55 e use-a para determinar a tabela-verdade completa. Em seguida, aplique as formas de onda mostradas na Figura 3.54 às entradas do circuito e desenhe a forma de onda de saída resultante.

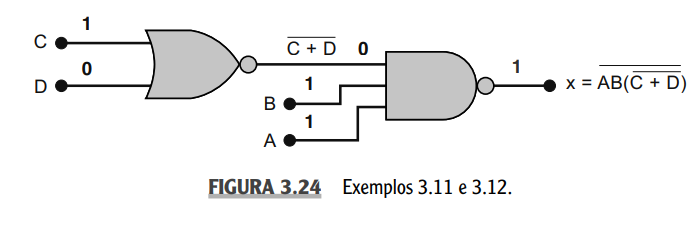


R:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

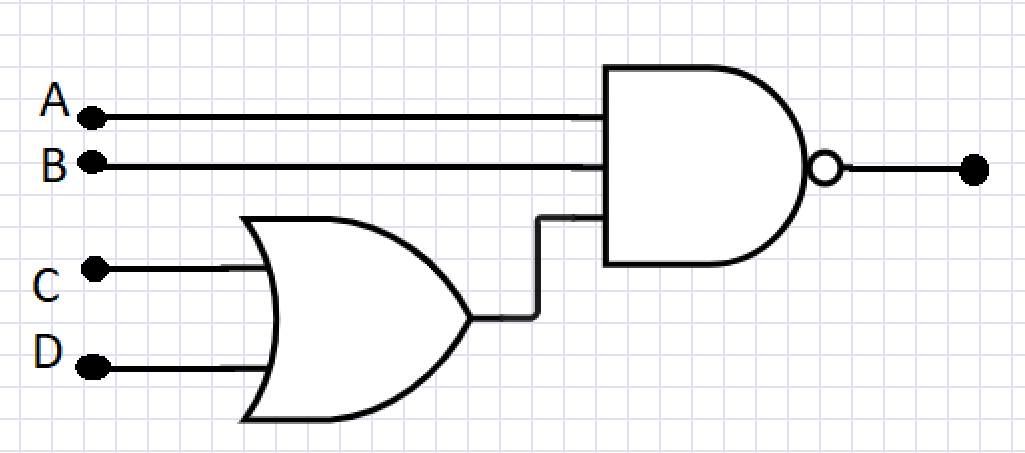
B 3.20 Determine a tabela-verdade para o circuito da Figura 3.24.



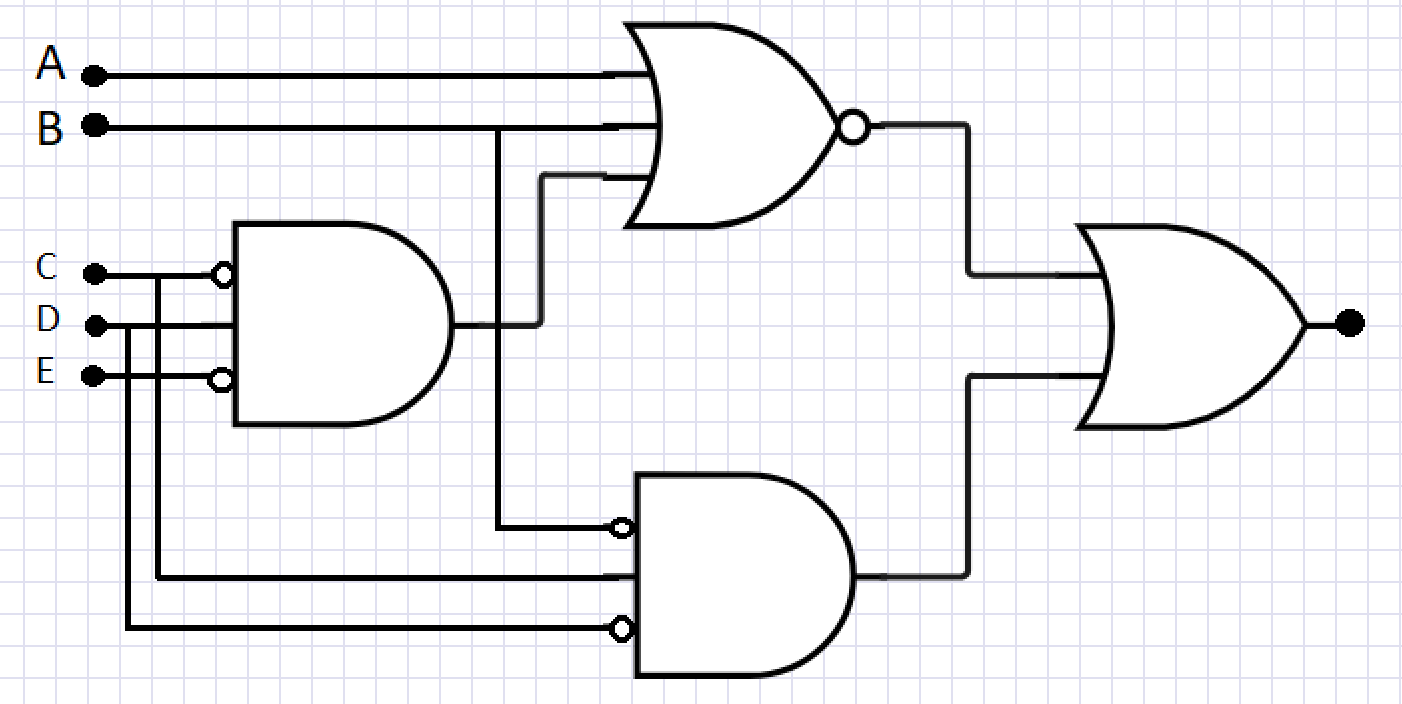
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

B 3.21 Modifique os circuitos construídos no Problema 3.16 para usar as portas NAND e NOR onde for apropriado.

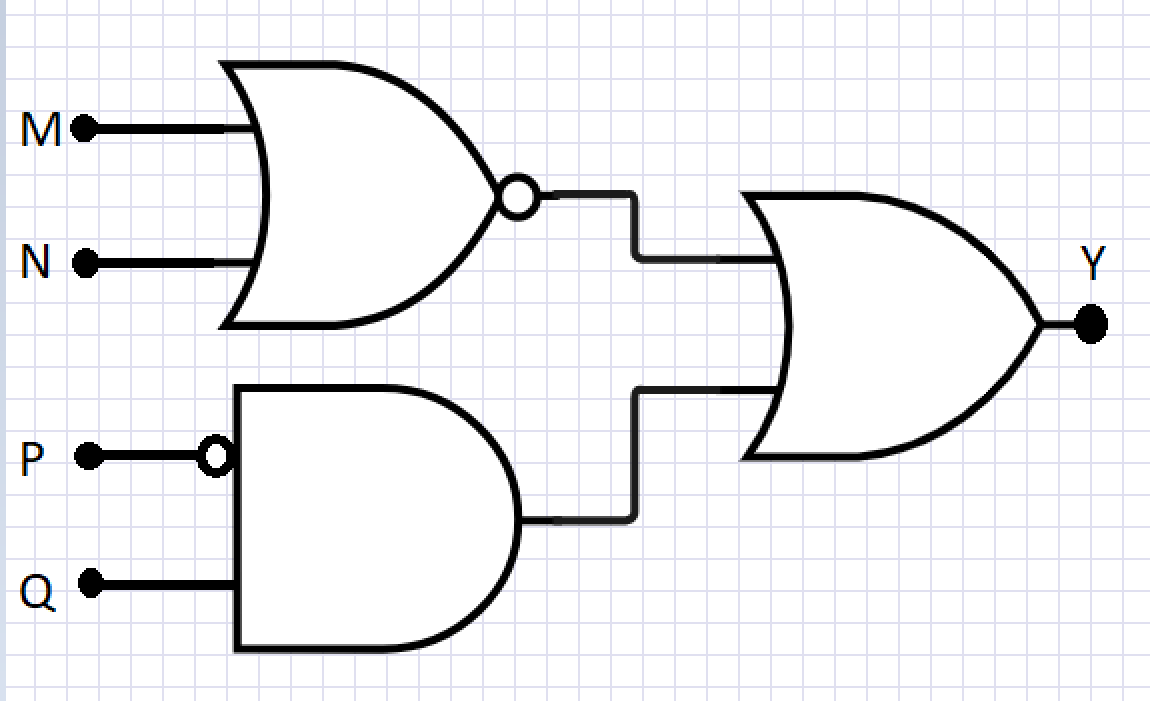
(a)\*



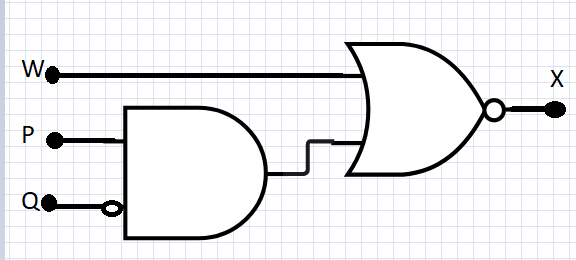
(b)\*



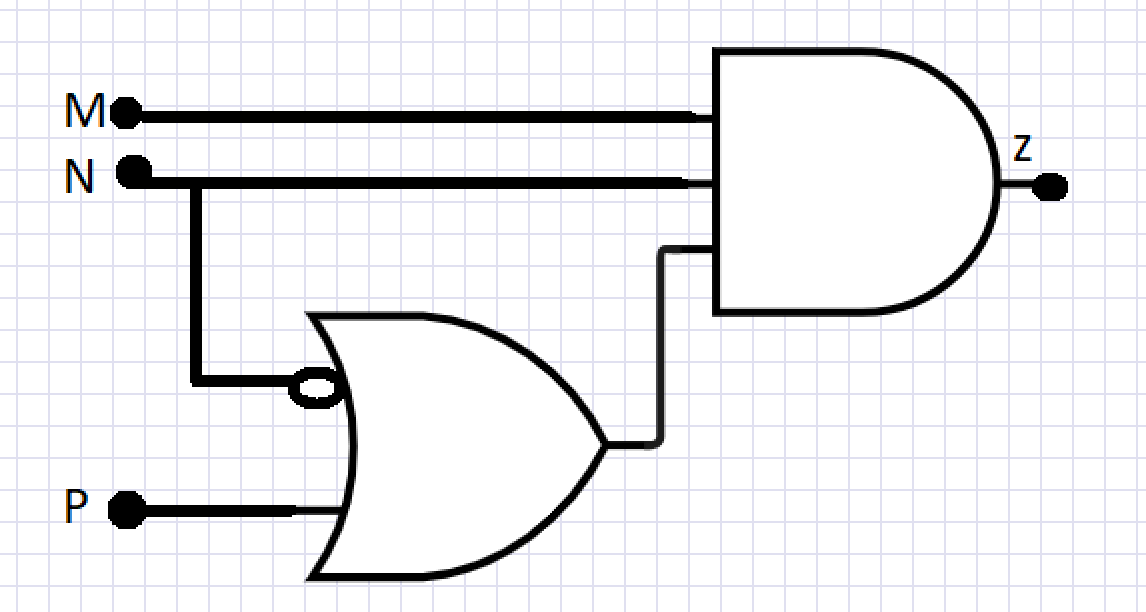
(c)



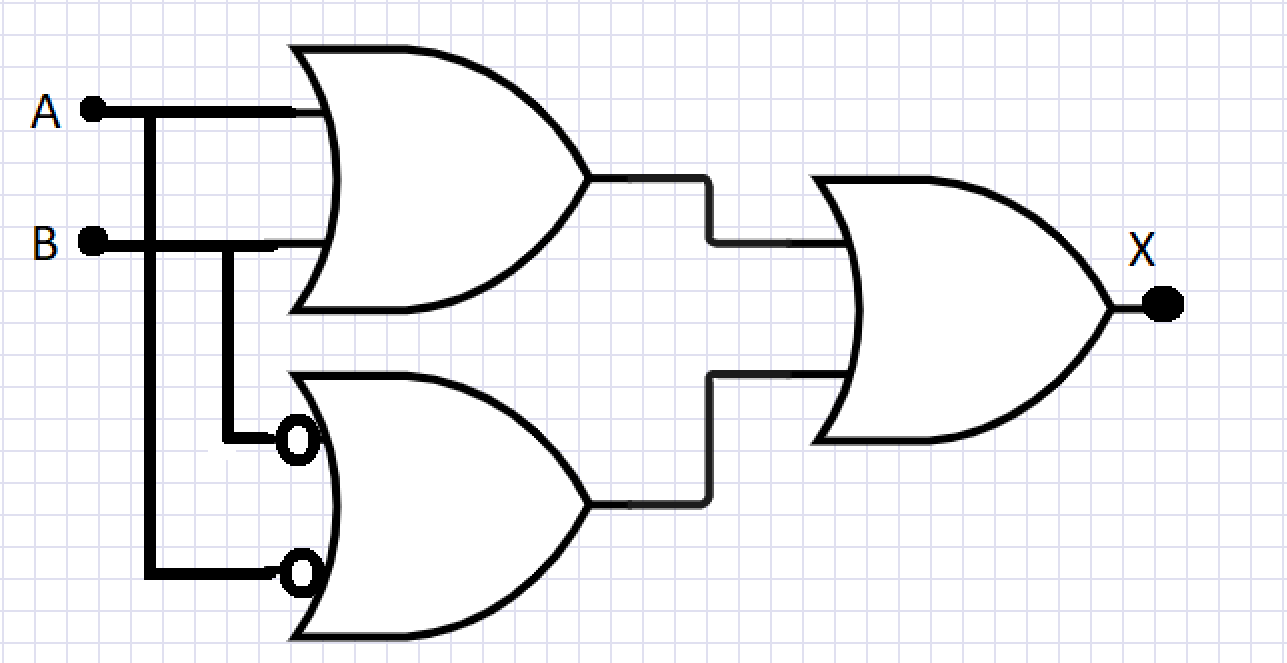
(d)



(e)



(f)



B 3.23\* EXERCÍCIOS DE FIXAÇÃO

Complete cada expressão.

(a)

(b)

(c)

(d)

(e)

(f)

(g)

(h)

(i)

(j)

C 3.24 (a)\* Simplifique a seguinte expressão usando os teoremas (13b), (3) e (4):

(b) Simplifique a seguinte expressão usando os teoremas (13a), (8) e (6):

# 

# **Parte II - Livro Thomas L. Floyd**

1. When the input to an inverter is LOW (0), the output is:

(a) HIGH or 0

(b) LOW or 0

(c) HIGH or 1

(d) LOW or 1

2. An inverter performs an operation known as:

(a) complementation

(b) assertion

(c) inversion

(d) both answers (a) and (c)

3. The output of an AND gate with inputs A, B and C is 0 (LOW) when

(a) A = 0, B = 0, C = 0

(b) A = 0, B = 1, C = 1

(c) both answers (a) and (b)

4. The output of an OR gate with inputs A, B and C is 0 (LOW) when

(a) A = 0, B = 0, C = 0

(b) A = 0, B = 1, C = 1

(c) both answers (a) and (b)

5. A pulse is applied to each input of a 2-input NAND gate. One pulse goes HIGH at t= 0 and goes back LOW at t = 1 ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

(a) It goes LOW at t = 0 and back HIGH at t = 3 ms.

(b) It goes LOW at t = 0.8 ms and back HIGH at t = 3 ms.

(c) It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms.

(d) It goes LOW at t = 0.8 ms and back LOW at t = 1 ms.

6. A pulse is applied to each input of a 2-input NOR gate. One pulse goes HIGH at t=0 and goes back LOW at t = 1 ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

(a) It goes LOW at t = 0 and back HIGH at t = 3 ms.

(b) It goes LOW at t = 0.8 ms and back HIGH at t = 3 ms.

(c) It goes LOW at t = 0.8 ms and back HIGH at t = 1 ms.

(d) It goes HIGH at t = 0.8 ms and back LOW at t = 1 ms.

7. A pulse is applied to each input of an exclusive-OR (XOR) gate. One pulse goes HIGH at t = 0 and goes back LOW at t = 1 ms. The other pulse goes HIGH at t = 0.8 ms and goes back LOW at t = 3 ms. The output pulse can be described as follows:

(a) It goes HIGH at t = 0 and back LOW at t = 3 ms.

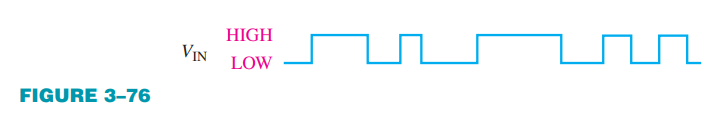
(b) It goes HIGH at t = 0 and back LOW at t = 0.8 ms.

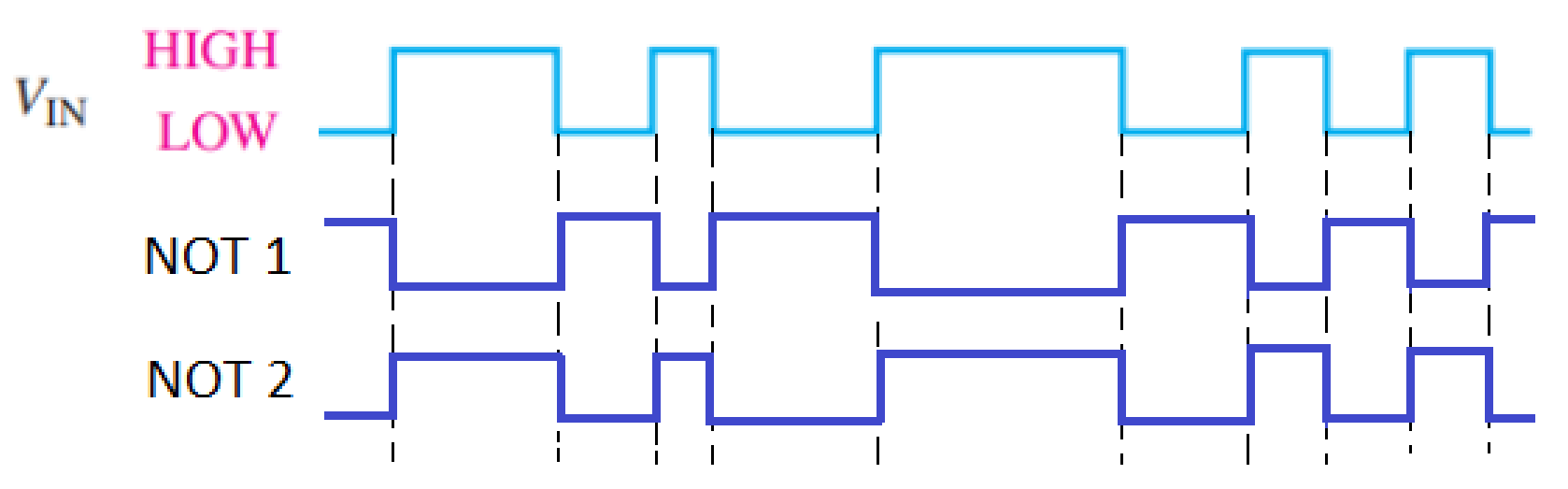
(c) It goes HIGH at t = 1 ms and back LOW at t = 3 ms.

(d) both answers (b) and (c)

Section 3-1:

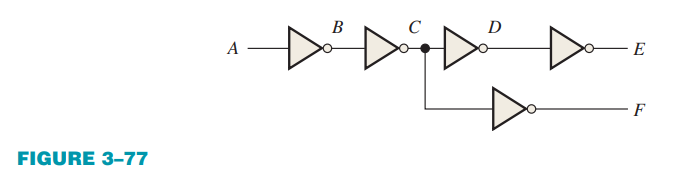
1. The input waveform shown in Figure 3–76 is applied to a system of two inverters connected in a series. Draw the output waveform across each inverter in proper relation to the input.

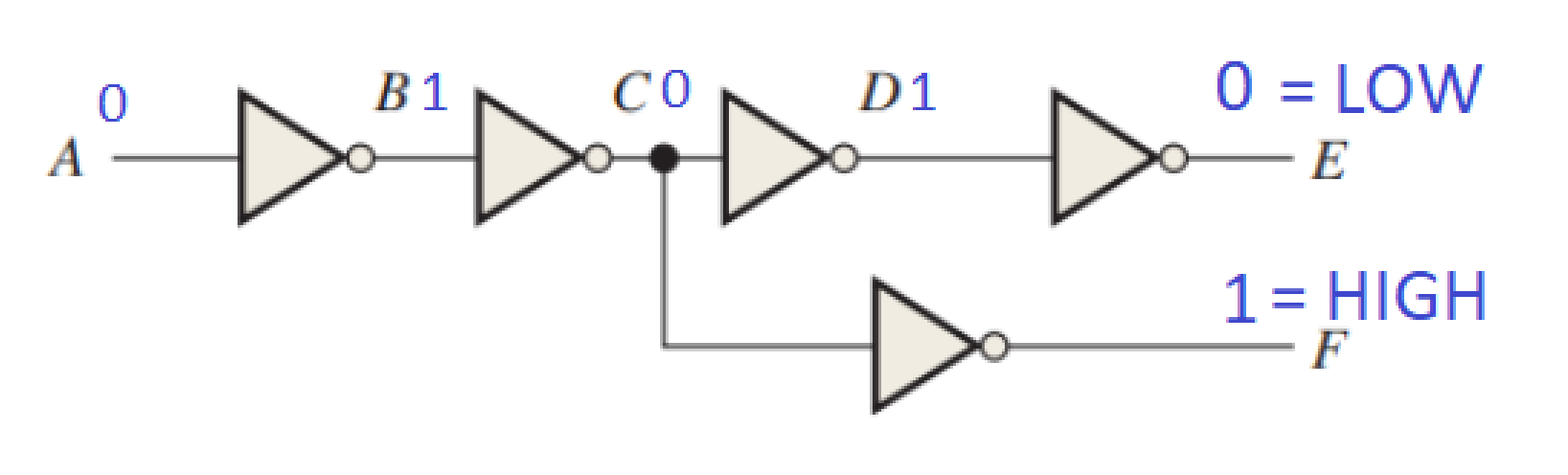




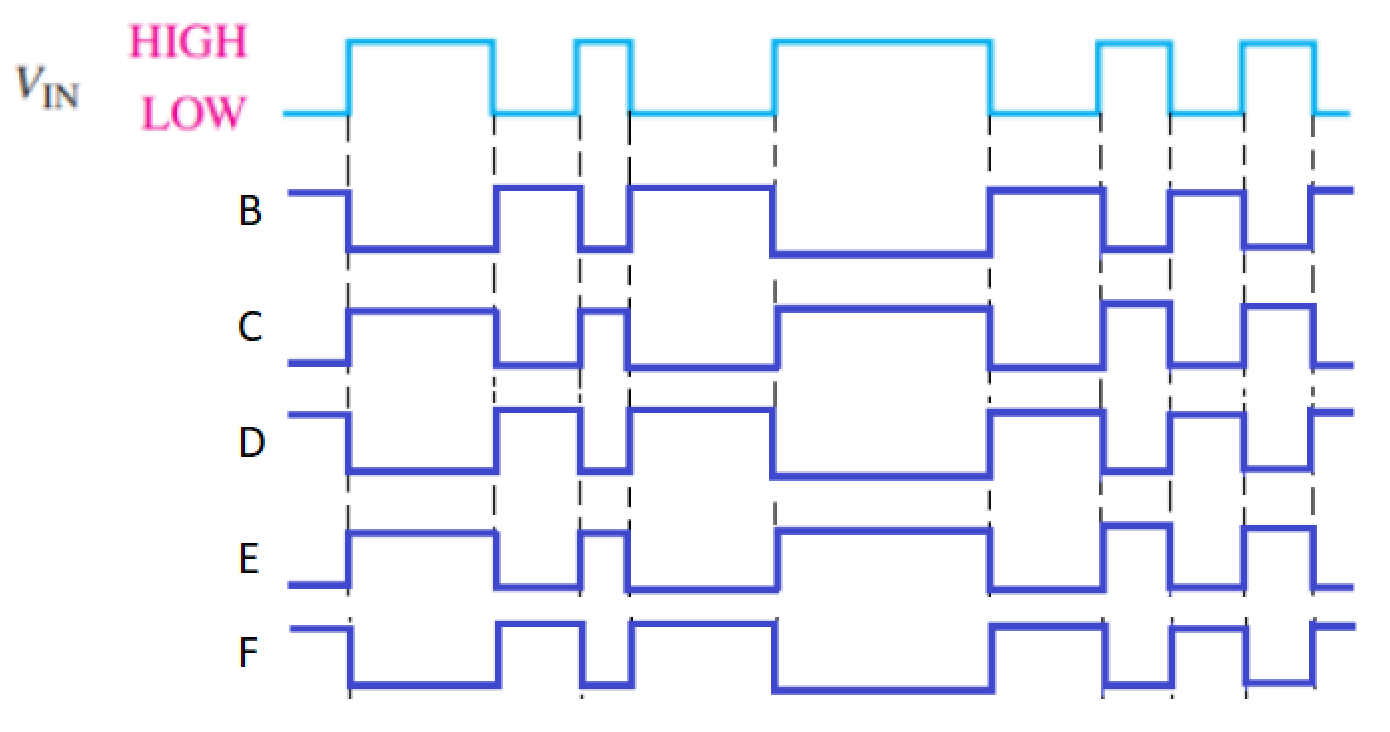
Ou seja, a onda resultante seria igual a onda original.

2. A combination of inverters is shown in Figure 3–77. If a LOW is applied to point A, determine the net output at points E and F.

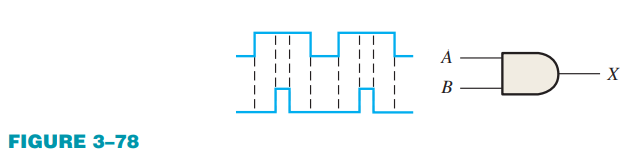


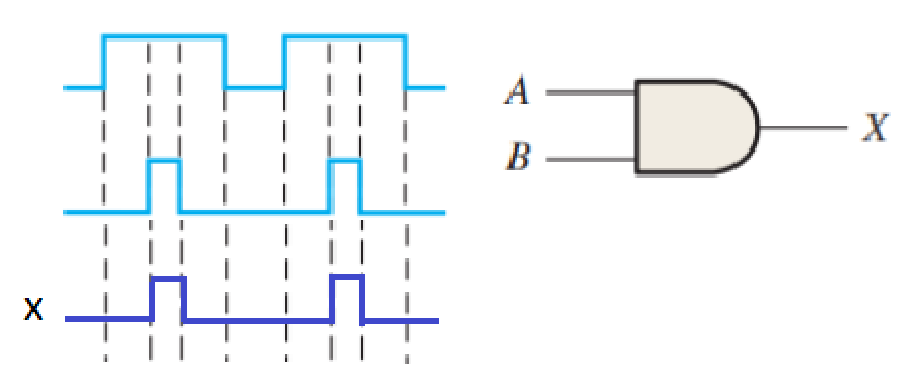


3. If the waveform in Figure 3–76 is applied to point A in Figure 3–77, determine the waveforms at points B through F.

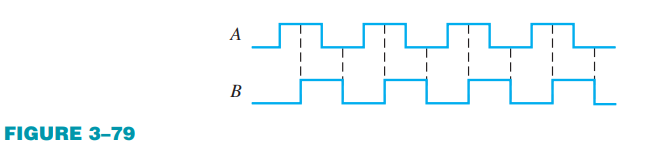


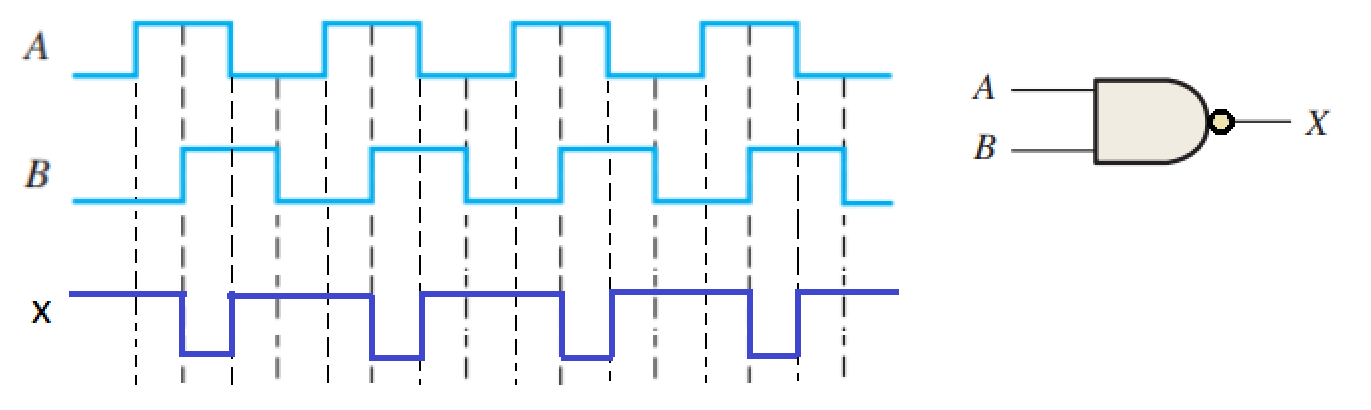
5. Determine the output, X, for a 2-input AND gate with the input waveforms shown in Figure 3–78. Show the proper relationship of output to inputs with a timing diagram.



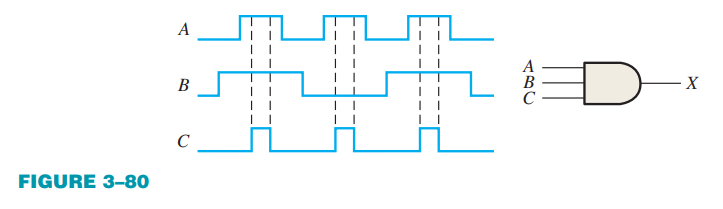


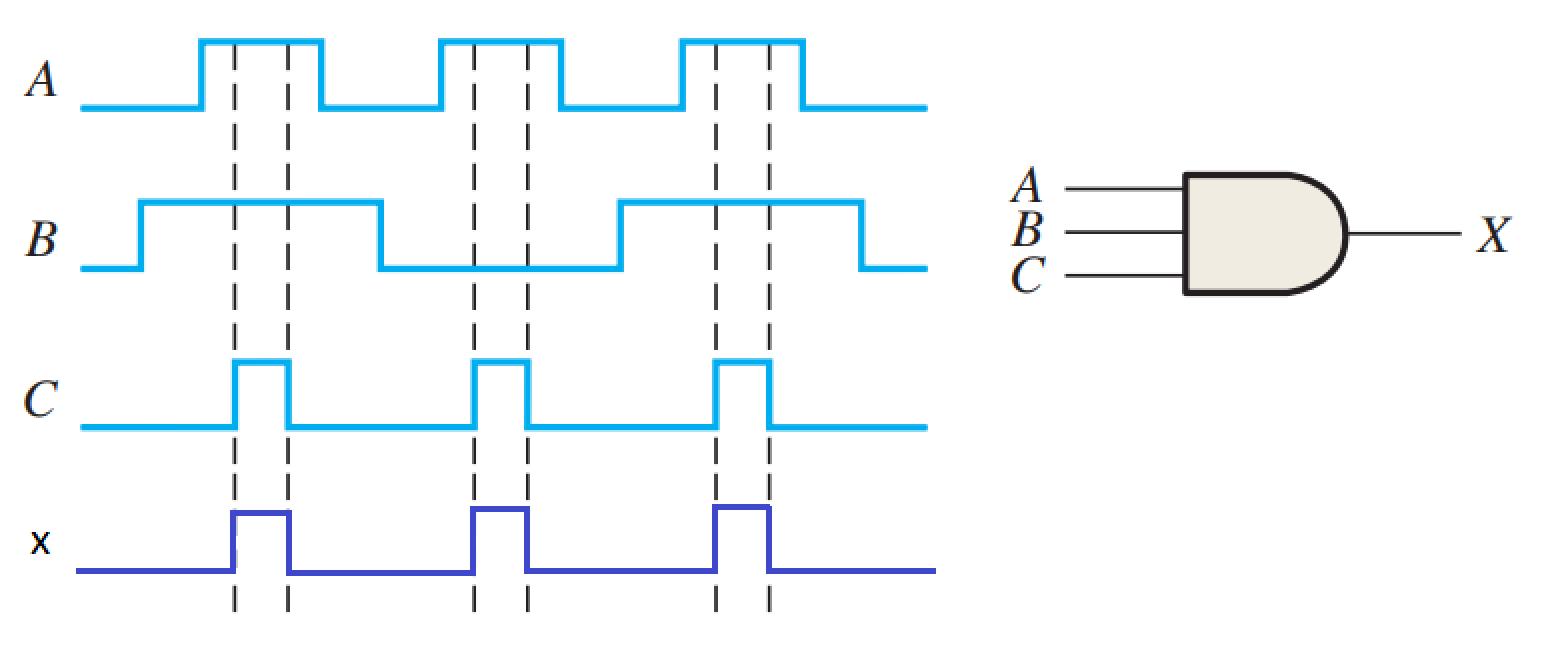
6. The waveforms in Figure 3–79 are applied to points A and B of a 2-input AND gate followed by an inverter. Draw the output waveform.



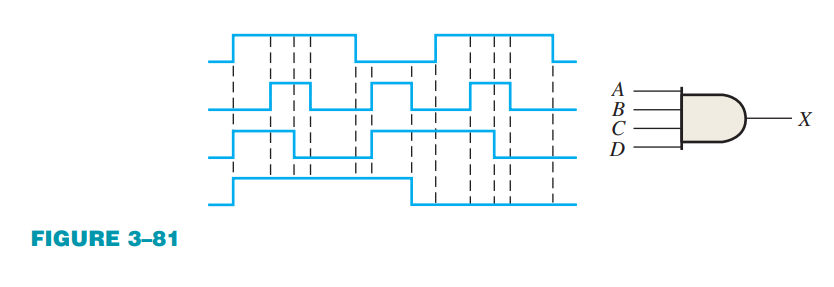


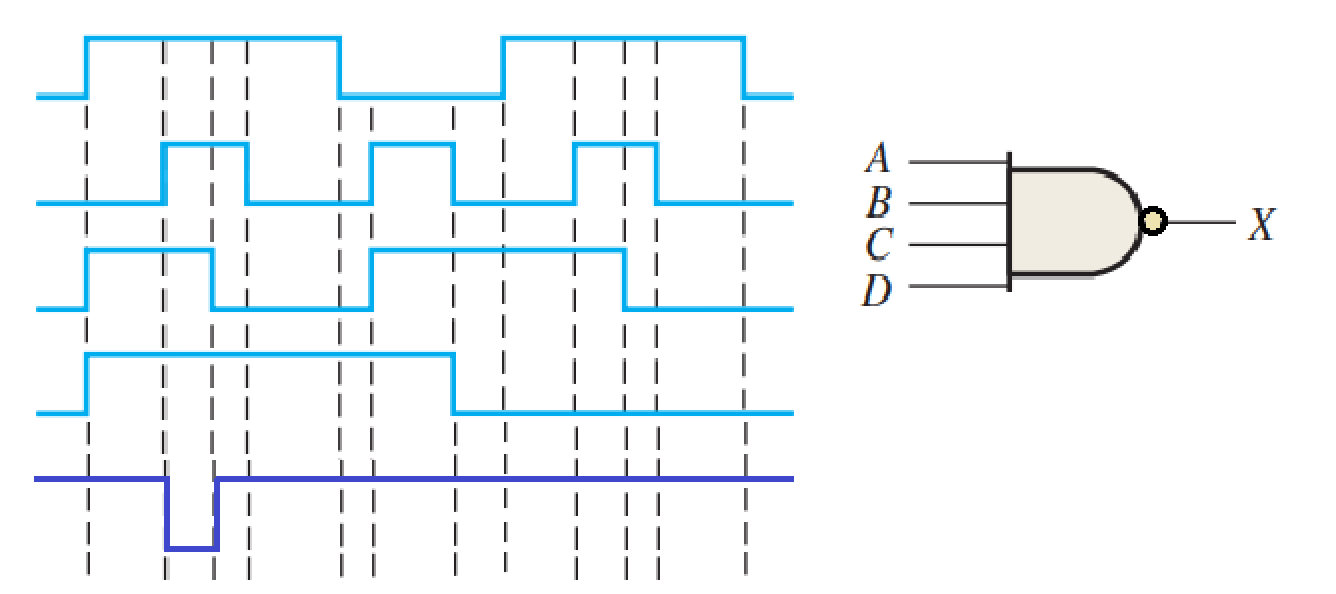
7. The input waveforms applied to a 3-input AND gate are as indicated in Figure 3–80. Show the output waveform in proper relation to the inputs with a timing diagram.





8. The input waveforms applied to a 4-input AND gate are as indicated in Figure 3–81. The output of the AND gate is fed to an inverter. Draw the net output waveform of this system.

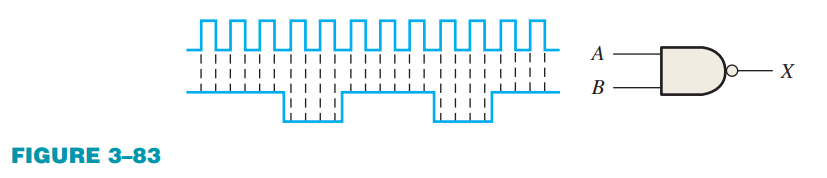


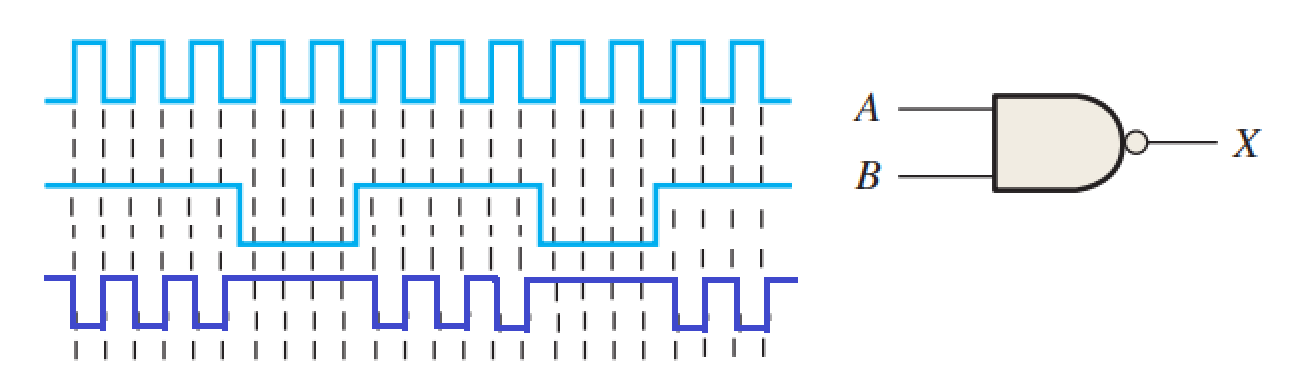


16. Show the truth table for a system of a 3-input OR gate followed by an inverter.

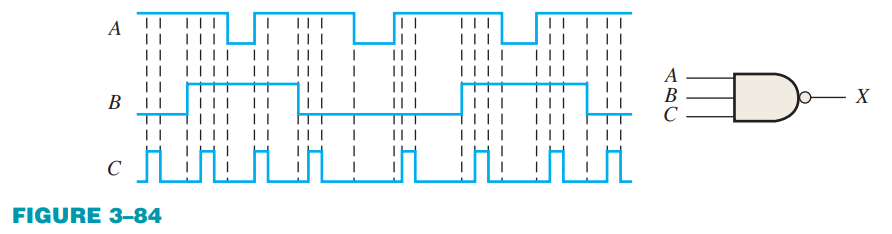
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |

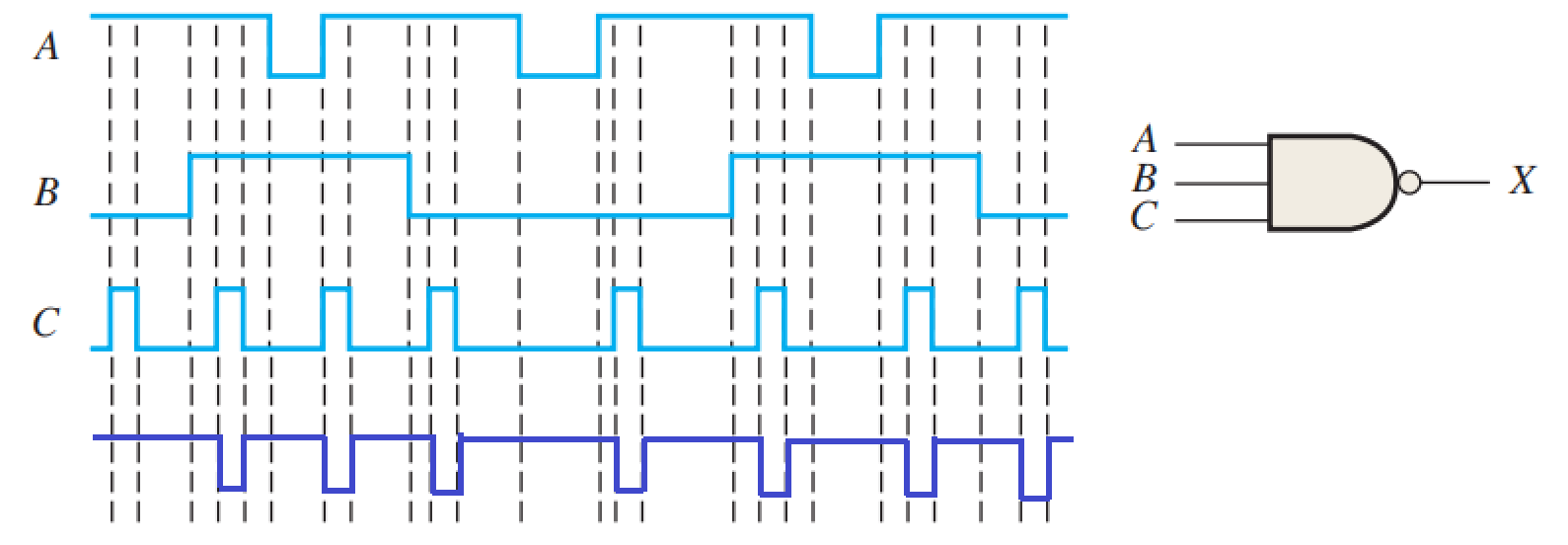
17. For the set of input waveforms in Figure 3–83, determine the output for the gate shown and draw the timing diagram.



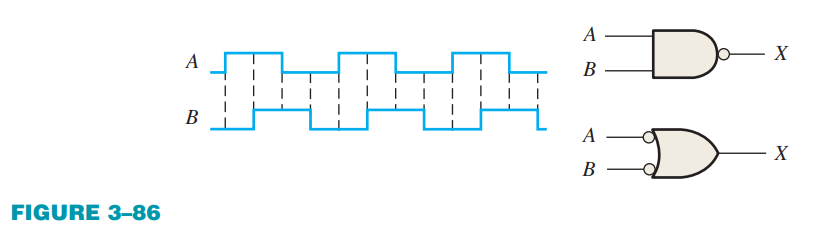


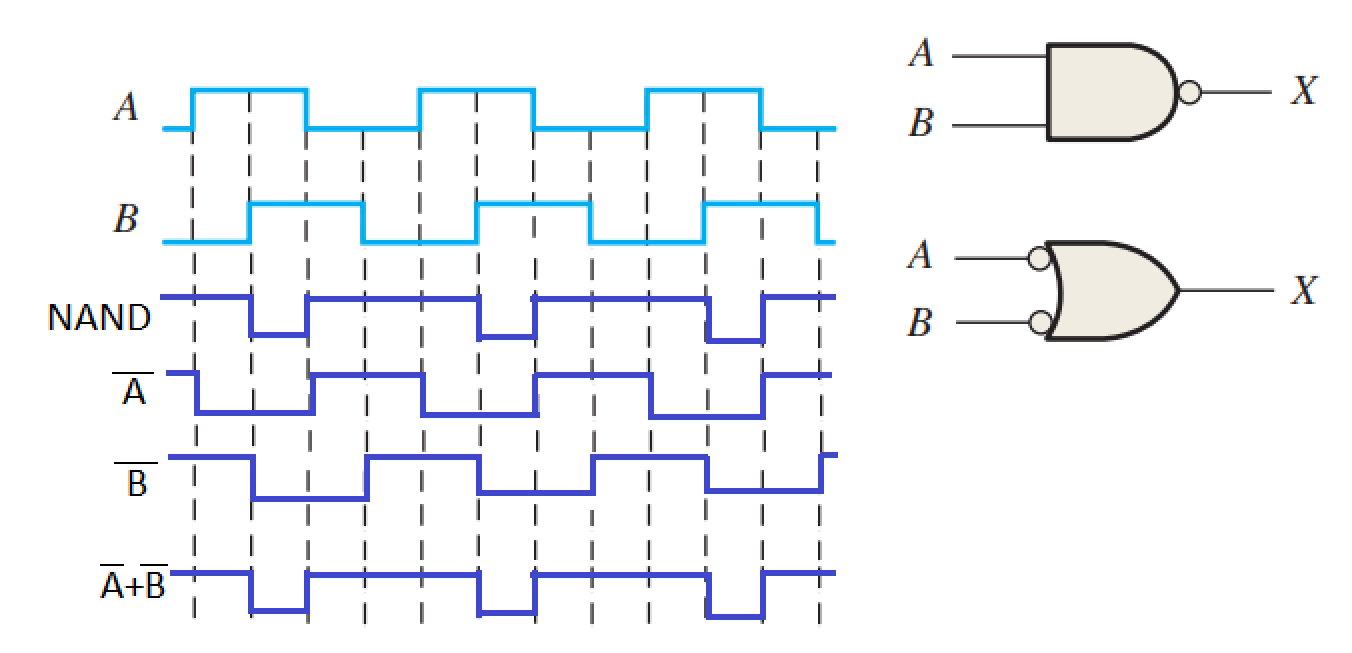
18. Determine the gate output for the input waveforms in Figure 3–84 and draw the timing diagram.



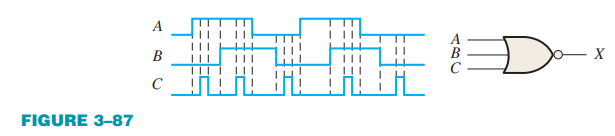


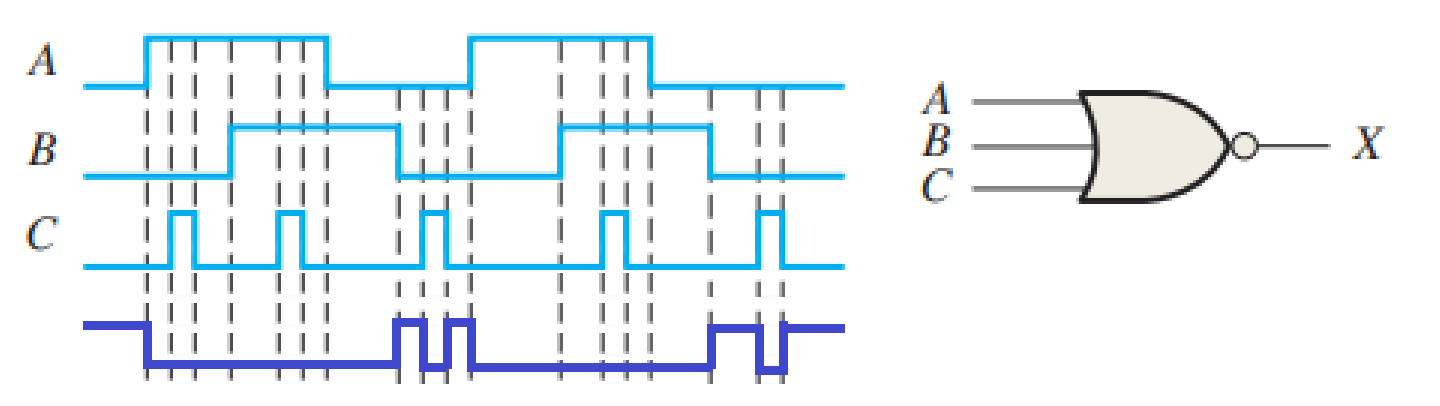
20. As you have learned, the two logic symbols shown in Figure 3–86 represent equivalent operations. The difference between the two is strictly from a functional viewpoint. For the NAND symbol, look for two HIGHs on the inputs to give a LOW output. For the negativeOR, look for at least one LOW on the inputs to give a HIGH on the output. Using these two functional viewpoints, show that each gate will produce the same output for the given inputs.



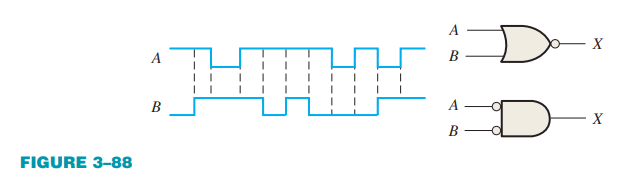


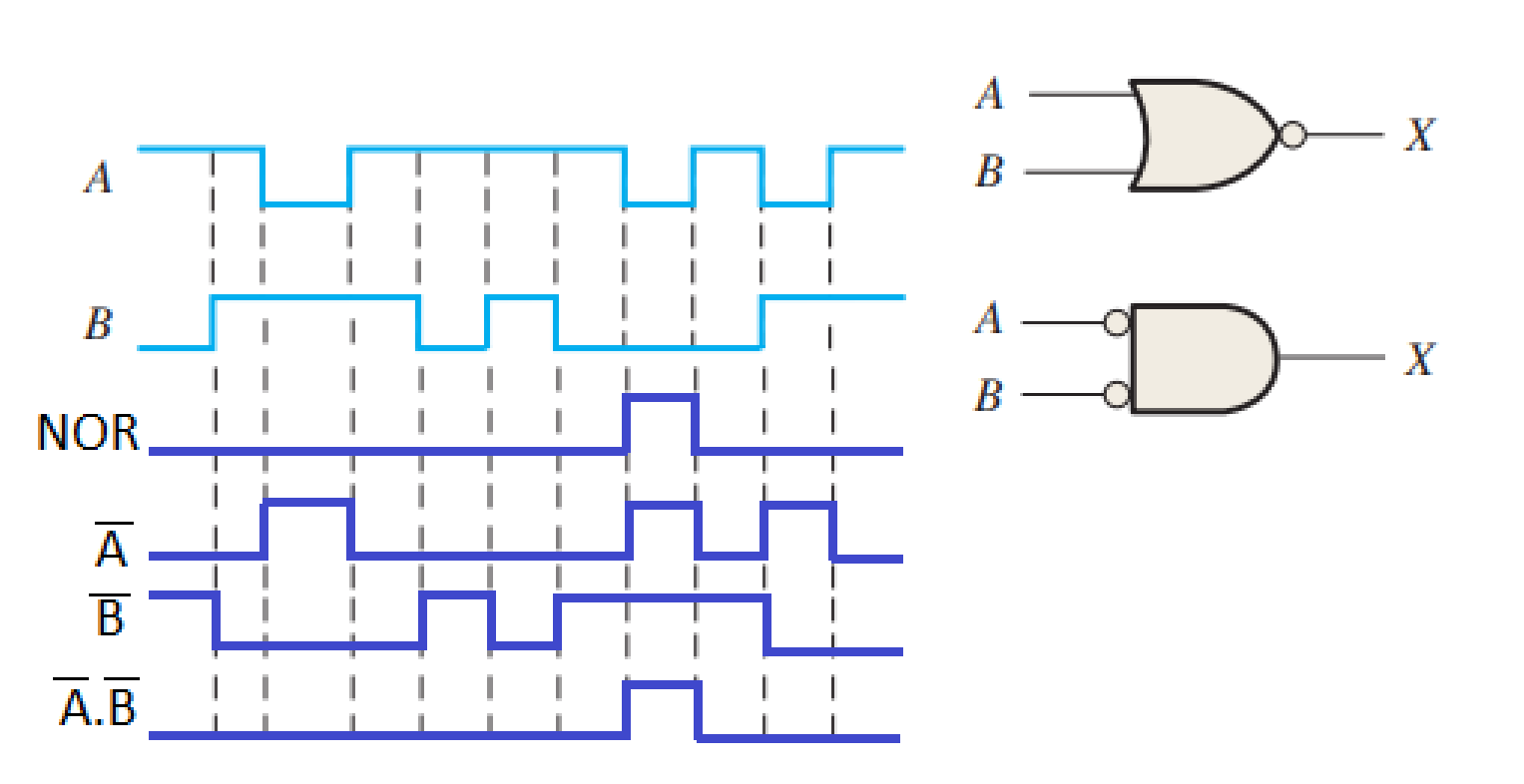
22. Determine the output waveform in Figure 3–87 and draw the timing diagram.





24. The NAND and the negative-OR symbols represent equivalent operations, but they are functionally different. For the NOR symbol, look for at least one HIGH on the inputs to give a LOW on the output. For the negative-AND, look for two LOWs on the inputs to give a HIGH output. Using these two functional points of view, show that both gates in Figure 3–88 will produce the same output for the given inputs.





25. How does an exclusive-OR gate differ from an OR gate in its logical operation?

R: Uma porta OR somente tem uma saída LOW quando todas as entradas são LOW, já uma porta XOR as entradas devem ser opostas para serem HIGH, caso contrário é LOW.

2. The Boolean expression is:

(a) a sum term

(b) a literal term

(c) an inverse term

(d) a product term

3. The Boolean expression is:

(a) a sum term

(b) a literal term

(c) an inverse term

(d) a product term

4. The domain of the expression is

(a) A and D

(b) B only

(c) A, B, C, and D

(d) none of these

5. According to the associative law of addition,

(a) A + B = B + A

(b) A = A + A

(c) (A + B) + C = A + (B + C)

(d) A + 0 = A

6. According to commutative law of multiplication,

(a) AB = BA

(b) A = AA

(c) (AB)C = A(BC)

(d) A0 = A

7. According to the distributive law,

(a) A(B + C) = AB + AC

(b) A(BC) = ABC

(c) A(A + 1) = A

(d) A + AB = A

8. Which one of the following is not a valid rule of Boolean algebra?

(a) A + 1 = 1

(b) AA = A

(c)

(d) A + 0 = A

9. Which of the following rules states that if one input of an AND gate is always 1, the output is equal to the other input?

(a) A + 1 = 1

(b) A + A = A

(c) A .A = A

(d) A .1 = A

10. According to DeMorgan’s theorems, the complement of a product of variables is equal to:

(a) the complement of the sum

(b) the sum of the complements

(c) the product of the complements

(d) answers (a), (b), and (c)

11. The Boolean expression X = (A + B)(C + D) represents:

(a) two ORs ANDed together

(b) two ANDs ORed together

(c) A 4-input AND gate

(d) a 4-input OR gate

12. An example of a sum-of-products expression is:

(a) A + B(C + D)

(b) AB + AC + ABC

(c) (A + B + C)(A + B + C)

(d) both answers (a) and (b)

13. An example of a product-of-sums expression is

(a) A(B + C) + AC

(b) (A + B)(A + B + C)

(c) A + B + BC

(d) both answers (a) and (b)

1. Using Boolean notation, write an expression that is a 0 only when all of its variables (A, B, C, and D) are 0s.

R:

2. Write an expression that is a 1 when one or more of its variables (A, B, C, D, and E) are 0s.

R:

3. Write an expression that is a 0 when one or more of its variables (A, B, and C) are 0s.

R:

4. Evaluate the following operations:

(a) 0 + 0 + 0 + 0 = 0

(b) 0 + 0 + 0 + 1 = 1

(c) 1 + 1 + 1 + 1 = 1

(d) 1 . 1 + 0 . 0 + 1 = 1

(e) 1 . 0 . 1 . 0 = 0

(f) 1 . 0 + 1 . 0 + 0 . 1 + 0 . 1 = 0

5. Find the values of the variables that make each product term 1 and each sum term 0.

(a)

R: A = B = C = 1

(b)

R: A = 1, B = C = 0

(c)

R: A = B = 0, C = 1

(d)

R: A = B = 0, C = 1

(e)

R: A = 1, B = C = 0

(f)

R: A = 0, B = C = 1

6. Find the value of X for all possible values of the variables.

(a) X = A + B + C

R: Se todos forem 0, x = 0. Se ao menos 1 for 1, x = 1.

(b) X = (A + B)C

R: A e, ou, B deve ser 1 e C 1, para x = 1. Se todos ou C 0, x = 0.

(c)

R: Para x = 1, B deve ser 0 e A 1. Para x = 0, B deve ser 1 e A e C qualquer valor.

(d)

R: Para x = 1, A ou B deve ser 1, ou se A ou B forem 0 e C for 1. Todas as outras combinações serão 0.

(e)

R: X só e somente só será 1, enquanto A e B terem valores diferentes.

7. Identify the law of Boolean algebra upon which each of the following equalities is based:

(a)

R: Comutativa

(b)

R: Associativa

(c)

R: Distributiva

8. Identify the Boolean rule(s) on which each of the following equalities is based:

(a)

R: Lei 9 =

(b)

R: Lei 8 = e Lei 3 =

(c)

R: Lei 5 =

(d)

R: Lei 6 = e Lei 4 =

(e)

R: Lei 10 =

(f)

R: Lei 10 =

9. Apply DeMorgan’s theorems to each expression:

(a)

R:

(b)

R:

(c)

R:

(d)

R:

(e)

R:

(f)

R:

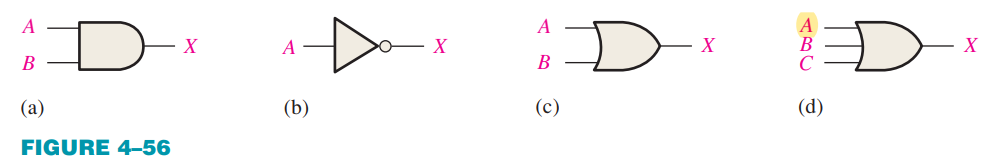
(g)

R:

(h)

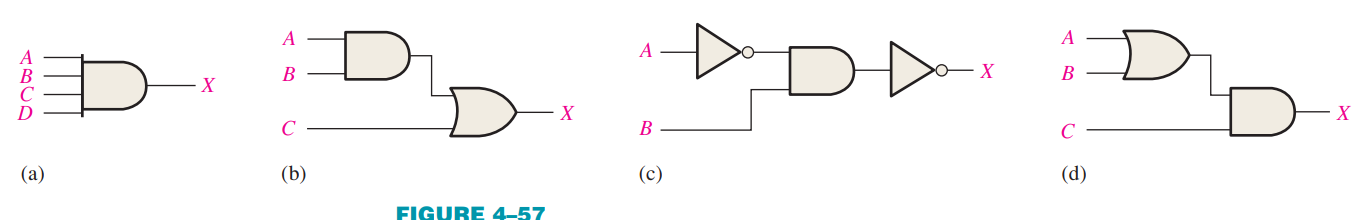
R:

12. Write the Boolean expression for each of the logic gates in Figure 4–56.



a) b) c) d)

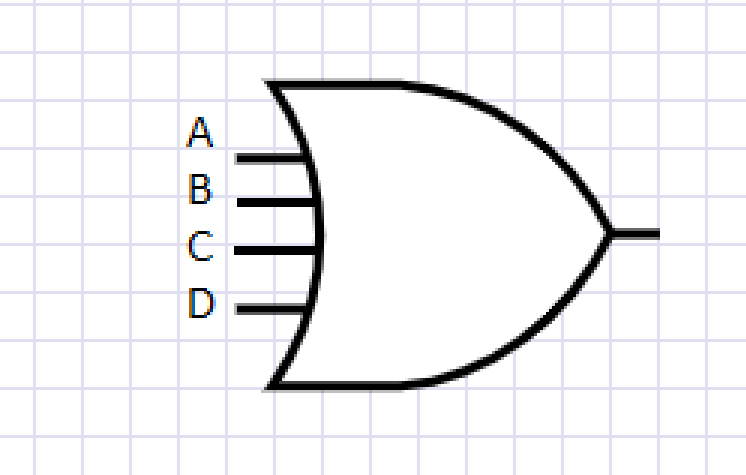
13. Write the Boolean expression for each of the logic circuits in Figure 4–57.



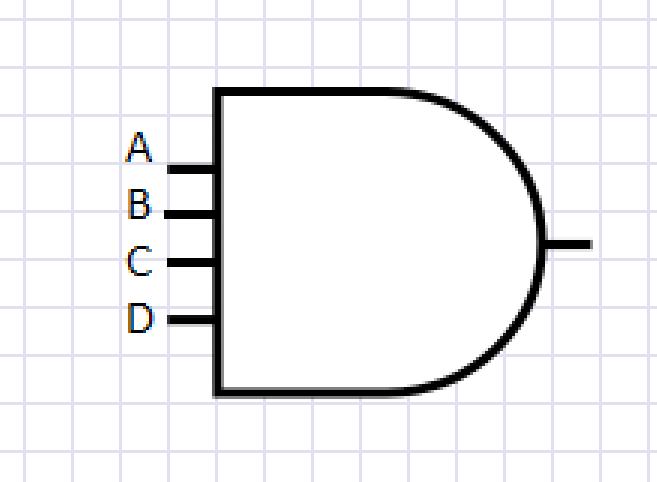
a) b) c) d)

14. Draw the logic circuit represented by each of the following expressions:

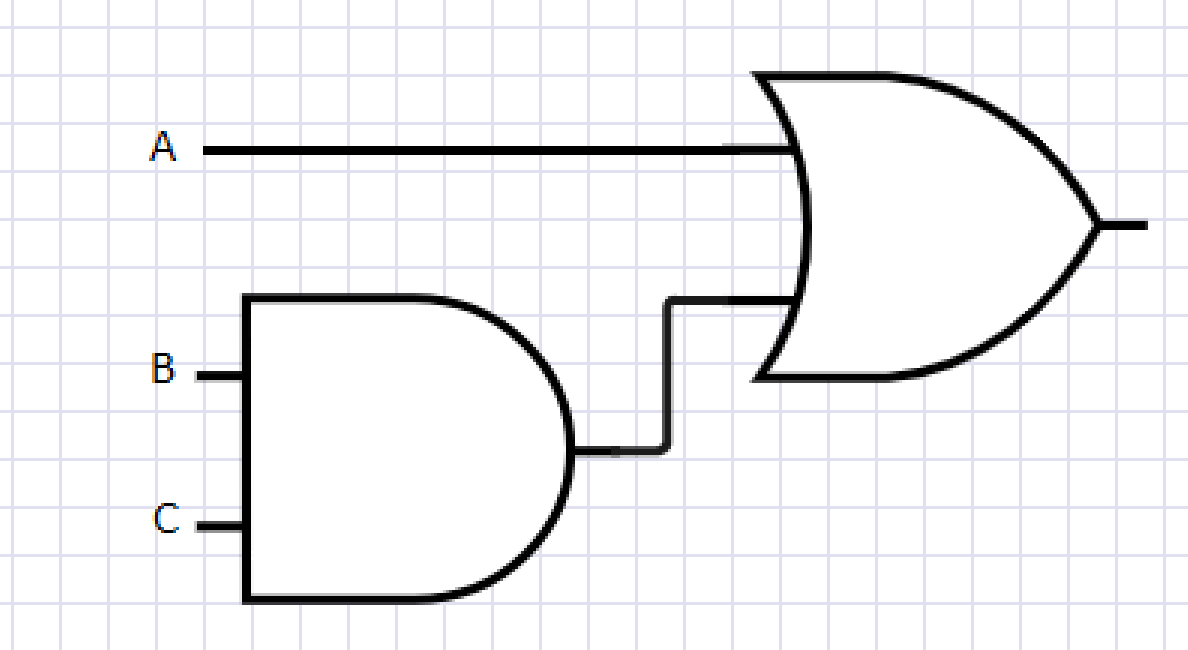
(a) A + B + C + D



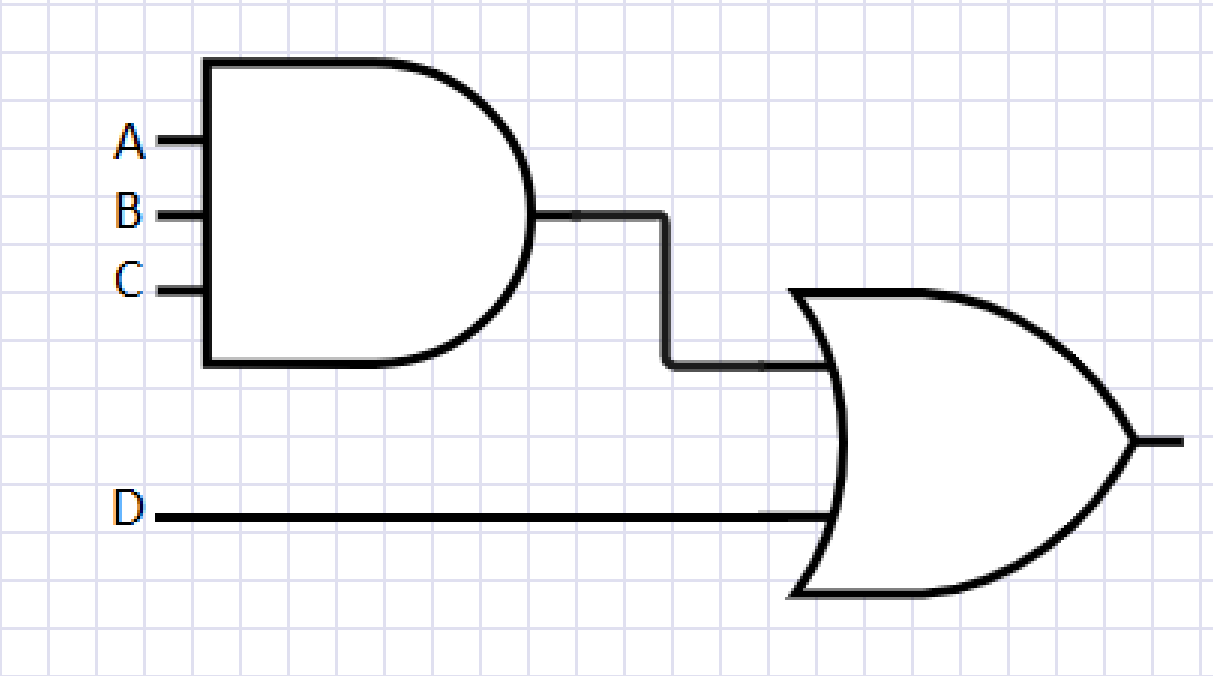
(b) ABCD



(c) A + BC

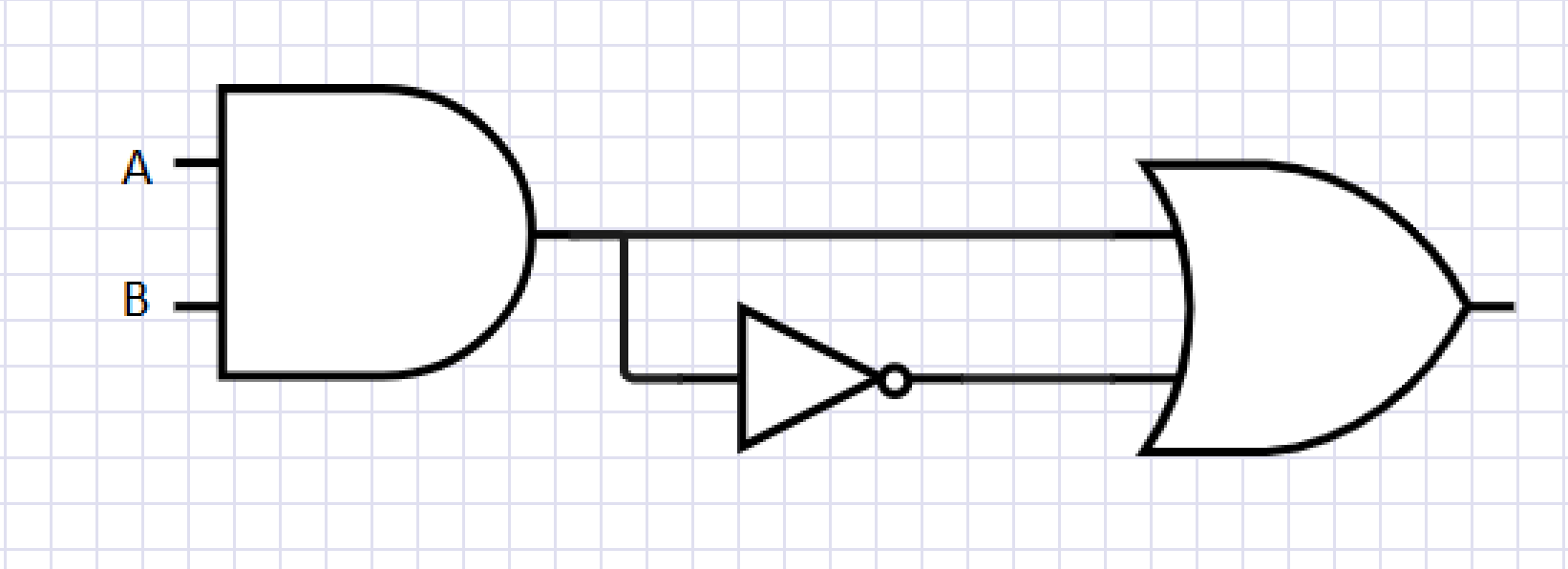


(d) ABC + D

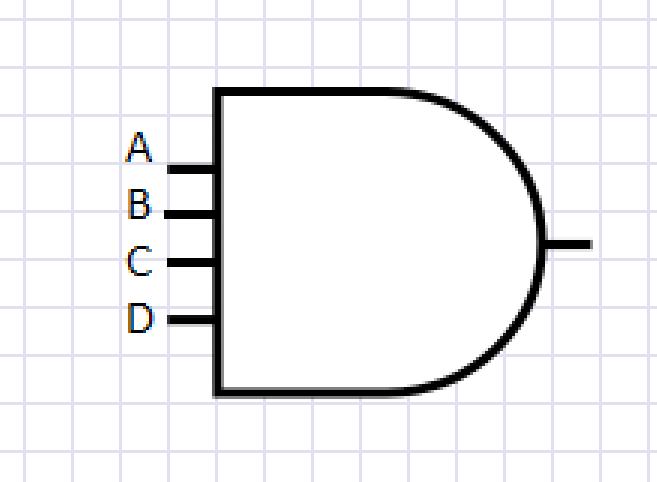


15. Draw the logic circuit represented by each expression:

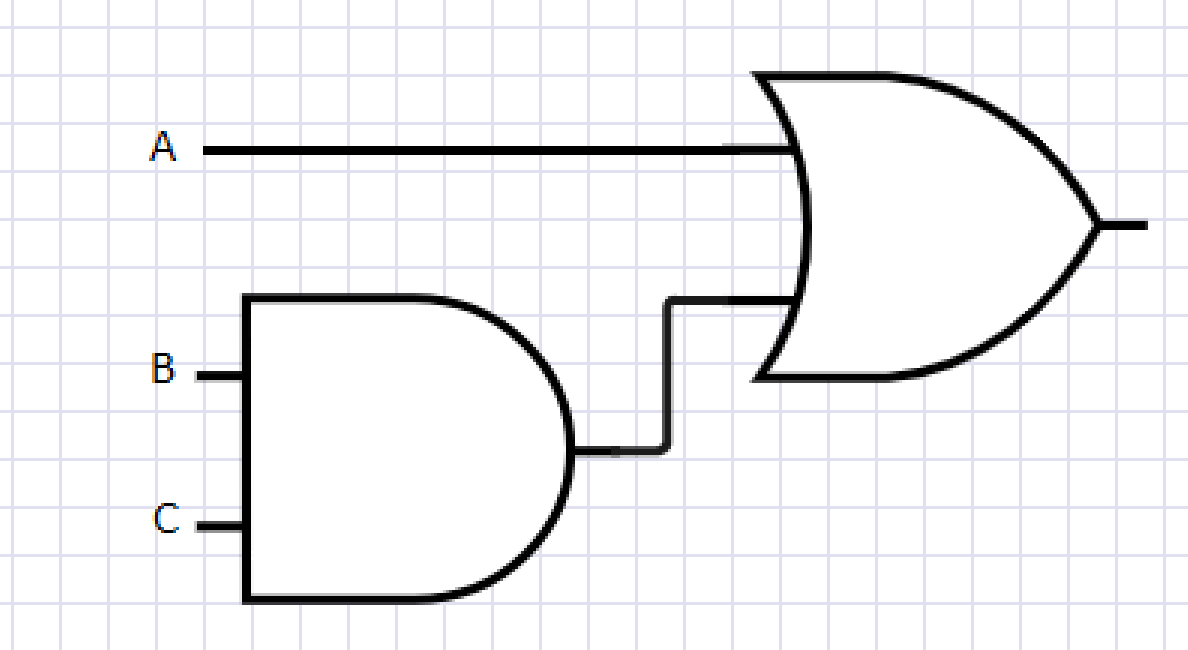
(a)



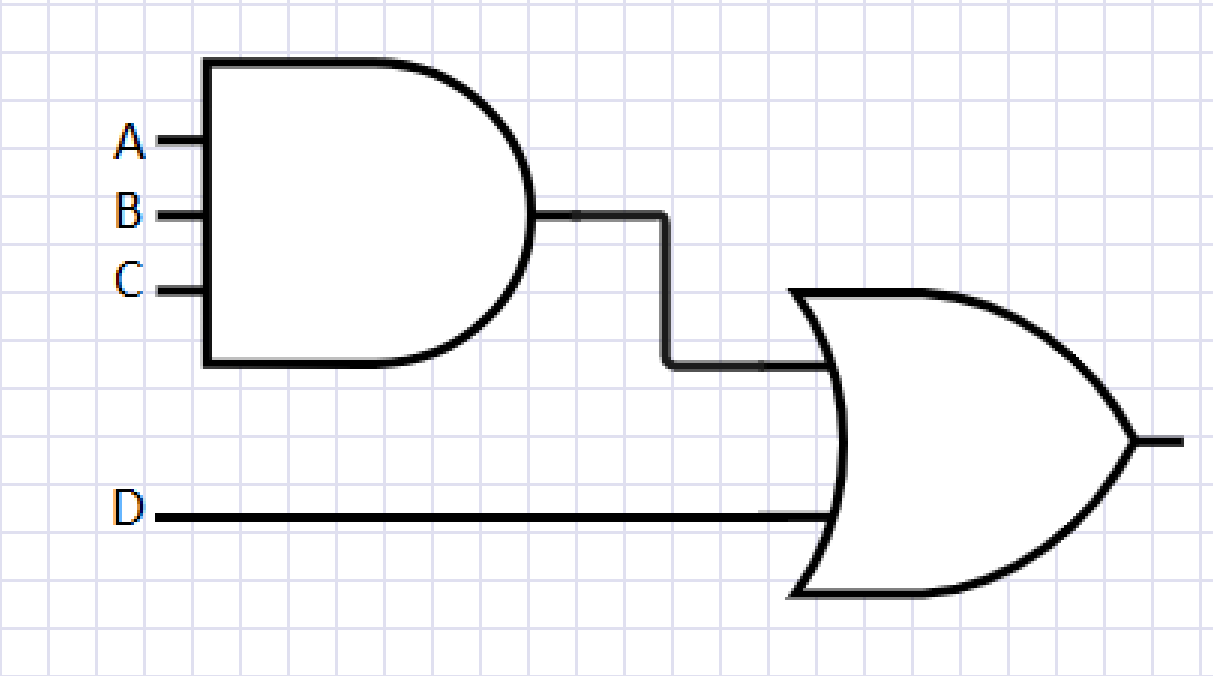
(b) ABCD



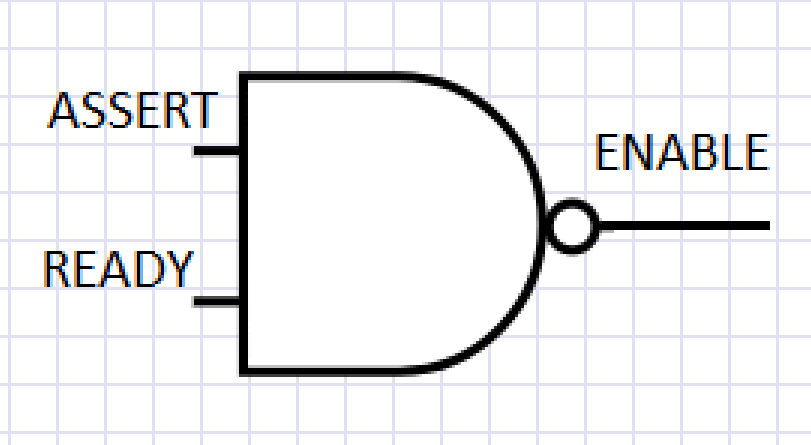
(c) A + BC



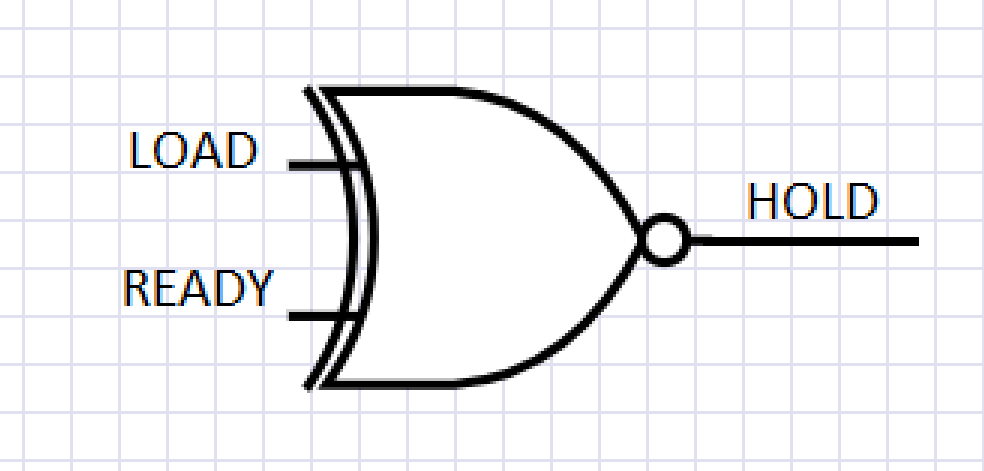
(d) ABC + D



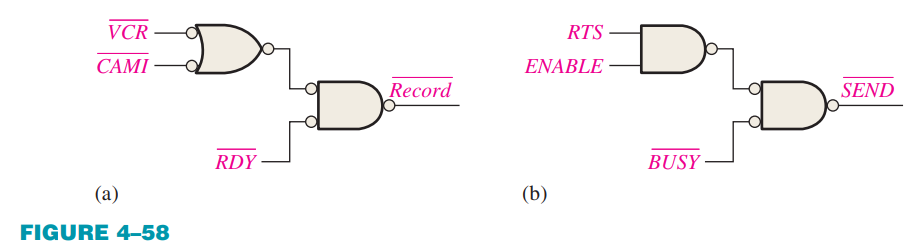
16. (a) Draw a logic circuit for the case where the output, ENABLE, is HIGH only if the inputs, ASSERT and READY, are both LOW.



(b) Draw a logic circuit for the case where the output, HOLD, is HIGH only if the input, LOAD, is LOW and the input, READY, is HIGH.



17. Develop the truth table for each of the circuits in Figure 4–58.



a)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

b)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 |

18. Construct a truth table for each of the following Boolean expressions:

(a) A + B + C

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

(b) ABC

|  |  |  |  |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

(c) AB + BC + CA

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

(d) (A + B)(B + C)(C + A)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

(e)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

19. Using Boolean algebra techniques, simplify the following expressions as much as possible:

(a) A(A + B)

AA + AB

A + AB

A

(b)

(c)

(d)

(e)

20. Using Boolean algebra, simplify the following expressions:

(a)

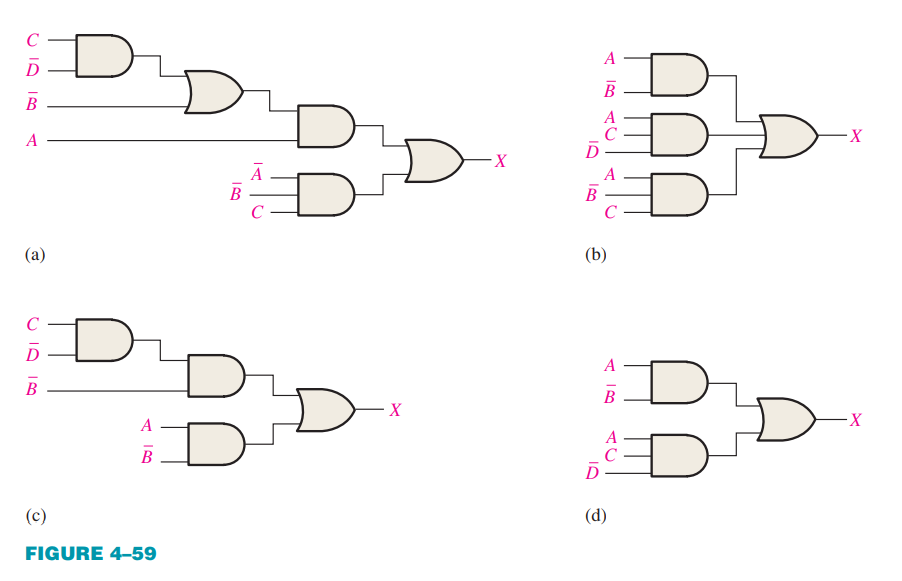
(b)

(c)

(d)

(e)

22. Determine which of the logic circuits in Figure 4–59 are equivalent.



R: A corresponde à D e B corresponde a C.

23. Convert the following expressions to sum-of-product (SOP) forms:

(a)

(b)

(c)

24. Convert the following expressions to sum-of-product (SOP) forms:

(a)

(b)

(c)

31. Develop a truth table for each of the following standard SOP expressions:

(a)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

b)

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

32. Develop a truth table for each of the following standard SOP expressions:

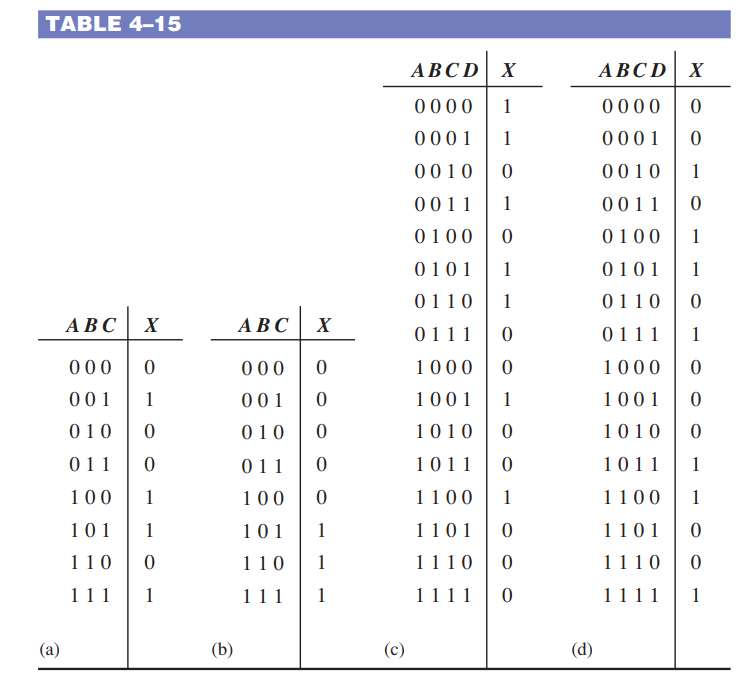
a)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

b)

|  |  |  |  |  |  |  |  |  | S |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

36. For each truth table in Table 4–15, derive a standard SOP and a standard POS expression.



1. SOP =

POS =

1. SOP =

POS =

1. SOP =

POS =

1. SOP =

POS =